XP152 MOSFET

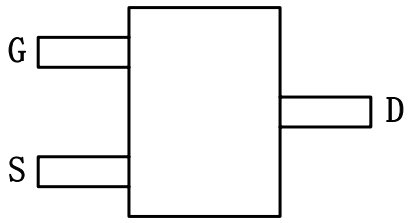
20V P-Channel Enhancement-Mode

VDS= -20V
RDS(ON), Vgs@-1.8V, Ids@-2.0A = 100mΩ@TYP
RDS(ON), Vgs@-4.5V, Ids@-2.8A = 71mΩ@TYP
RDS(ON), Vgs@-2.5V, Ids@-2.0A = 83mΩ@TYP

Features

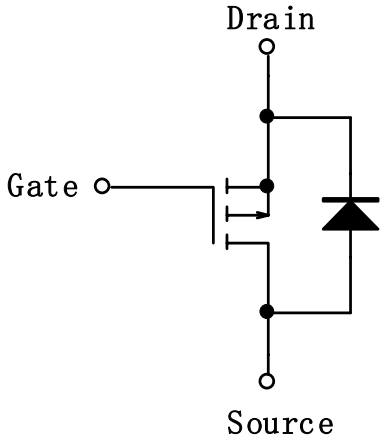
Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance

SOT- 23 / SOT-323 / SOT-353



Top View

Internal Schematic Diagram



P-Channel MOSEFT

Maximum Ratings and Thermal Characteristics (T_A= 25℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current [1)]		I_D	-2.2	A
Pulsed Drain Current [2)]		I_{DM}	-8	
Maximum Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=75℃		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	℃
Junction-to-Ambient Thermal Resistance (PCB mounted)[3)]		$R_{\theta JA}$	140	W/℃

Note: 1. Fused current that based on wire numbers and diameter
2. Repetitive Rating: Pulse width limited by the maximum junction temperature
3. 1-in^2 2oz Cu PCB board

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250uA	20	--	--	V
Drain-Source On-Stage Resistance	R_{DS}(on)	V_{GS} = -4.5V, I_D = -2.8A	--	71.0	100.0	mΩ
Drain-Source On-Stage Resistance	R_{DS}(on)	V_{GS} = -2.5V, I_D = -2.0A	--	83.0	150.0	
Drain-Source On-Stage Resistance	R_{DS}(on)	V_{GS} = -1.8V, I_D = -2.0A	--	100.0	170.0	
Gate Threshold Voltage	V_{GS}(th)	V_{DS} = V_{GS}, I_D = 250uA	-0.45	-0.61	-0.9	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -9.6V, V_{GS} = 0V	--	--	1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ±8V, I_{DS}=0uA	--	--	±100	nA
Dynamic[3)]						
Total Gate Charge	Q_g	V_{DS} = -6V, I_D = -2.8A V_{GS} = -4.5V	--	--	--	nC
Gate-Source Charge	Qg_s		--	--	--	
Gate-Drain Charge	Q_{gd}		--	--	--	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6V, R_L = 6Ω I_D = -1A, V_{GEN} = -4.5V R_G = 6Ω	--	--	--	ns
Turn-On Rise Time	t_r		--	--	--	
Turn-Off Delay Time	$t_{d(off)}$		--	--	--	
Turn-Off Fall Time	t_f		--	--	--	
Input Capacitance	C_{iss}	V_{DS} = -6V, V_{GS} = 0V f=1.0MHz	--	--	--	pF
Output Capacitance	C_{oss}		--	--	--	
Reverse Transfer Capacitance	C_{rss}		--	--	--	
Source-Drain Diode						
Max. Diode Forward Current	I_S	--	--	--	1.6	A
Diode Forward Voltage	V_{SD}	I_S = -1.6A, V_{GS} = 0V	--	-0.75	--	V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%

3. Guaranteed by design; not subject to production testing