TTP250x
Product
Specification

1. Introduction

TTP250 是一顆專爲電容式觸控 1~8 個按鍵而作的低成本 ASSP IC。TTP250 提供直接輸出方式，讓使用者能夠輕易的上手並且能簡單的應用在自己的系統上。

2. Features

- 操作電壓：2.0V ~ 5.5V
- 可提供 1~8 個 Touch Pad 選擇
- Provides sleep mode for power saving request (<5uA@3V)
- 依操作環境需求，每一 KEY 可各自經由 option 選擇不同靈敏度及不同的 De-bounce time
- Offers key-stuck release time interval selection (5 sec~ 90 sec)
- Provide direct output mode and Tontek serial mode
- 包裝形式 ：SKINNY DIP/SOP/SSOP/QFN 24 PIN
  DIP/SOP/SSOP/TSSOP/QFN 20 PIN
  DIP/SOP/SSOP/QFN 16 PIN
  DIP/SOP 8 PIN

3. Option Description

- LVR function (active Voltage 2.0~3.5V)
  LVR function 定義 LVR function 啓動或關閉。LVR 的啓動電壓爲 3.5V 以下。選項選擇 enable 時會開啓 LVR (Low Voltage Reset)功能。但是若 option 選擇 sleep mode enable 時,進入 sleep 時程式會自動關閉 LVR 功能以達到省電效果。選項選擇 disable 時會關閉 LVR 的功能。若客戶工作電壓爲 5V 且並不需使用到 LVR 功能或有省電考量者也請選擇 disable。option default is disable。

- Output Type
  Output Type 定義當有 KEY 被偵測到時的輸出模式。目前有 Direct Mode 及 Serial Mode 可供選擇。Key Type 選擇 Multi-key 時，提供 Direct Mode 及 Serial Mode 兩種輸出模式，選擇 single-key (strength)或 single-key (sequence)時，僅提供 Direct Mode 模式。所以當選擇到 serial mode 時，Key Type 會變換到 multi-key 而且不可選。

- Serial Mode output
  當 Output Type 選擇 Serial mode output 時，此選項才會出現。當選擇 2-wire(TT)或 3-wire(TT)時，若有偵測到 KEY 被按住時，IC 會依照 Tontek 公司 2-wire 或 3-wire serial output 的 protocol 方式，把偵測到的 KEY 輸出。其中 TPO0 爲 CK-S，TPO1 爲 DO-S，TPO2 爲 CSB-S。詳細說明請參考 TT serial interface protocol。

- Output active level
  選擇 Output Pin 的 Output active level．若選擇 Active Low-CMOS 時，若没有 KEY 被偵測到時輸出 Hi，若被偵測到時輸出 Low。若選擇 Active High-CMOS 時，若没有 KEY 被偵測到時輸出 Low，若 KEY 被偵測到時輸出 Hi。若選擇 Active Low-Open Drain 時，若没有 KEY 被偵測到時輸出 Tri-state，若 KEY 被偵測到時輸出 Low。若選擇 Active High- Open Source 時，若没有 KEY 被偵測到時輸出 Tri-state，若 KEY 被偵測到時輸出 Hi。此 option 僅有在 Output Type 選擇 Direct mode output 時，此選項才會出現。Default is Active Low-CMOS。

- Key Type
  Key Type 定義當有數個 KEY 同時被按住時的處理方式。當選擇 multi-key 時，若是同時有數個 KEY 被按住時，會同時承認每個被按住的 KEY。當選擇 single-key(strength)時，若是同時有數個 KEY 被按住時，只會承認其中感應到最大的一個 KEY，其他 KEY 均爲壓抑住。若每一 KEY 的感應效果相同時，則都不會被承認。當選擇 single-key(sequence) 時，若是同時有數個 KEY 被按住時，只會承認最早被感應到的一個 KEY，並且停在這一 KEY 上，直到 KEY 被 release 後才繼續 scan 行爲。Default is multi-key。

- Sleep mode
  選擇 IC 操作的模式。當選擇 disable 時, IC 會持續全速執行，進行 KEY 偵測。當選擇 enable 時，在指定的一段時間没有 KEY 被偵測到時，IC 會進入省電模式，但仍會繼續執行 KEY 偵測。當有 KEY 被 detect 且 wakeup 後，IC 會等到連續一段時(Refresh Update Time define valule)都没 KEY 被 detect，時才會再次進入 Sleep Mode。Default is disable。

4. Tontek Serial output protocol

3 wires serial interface single mode:

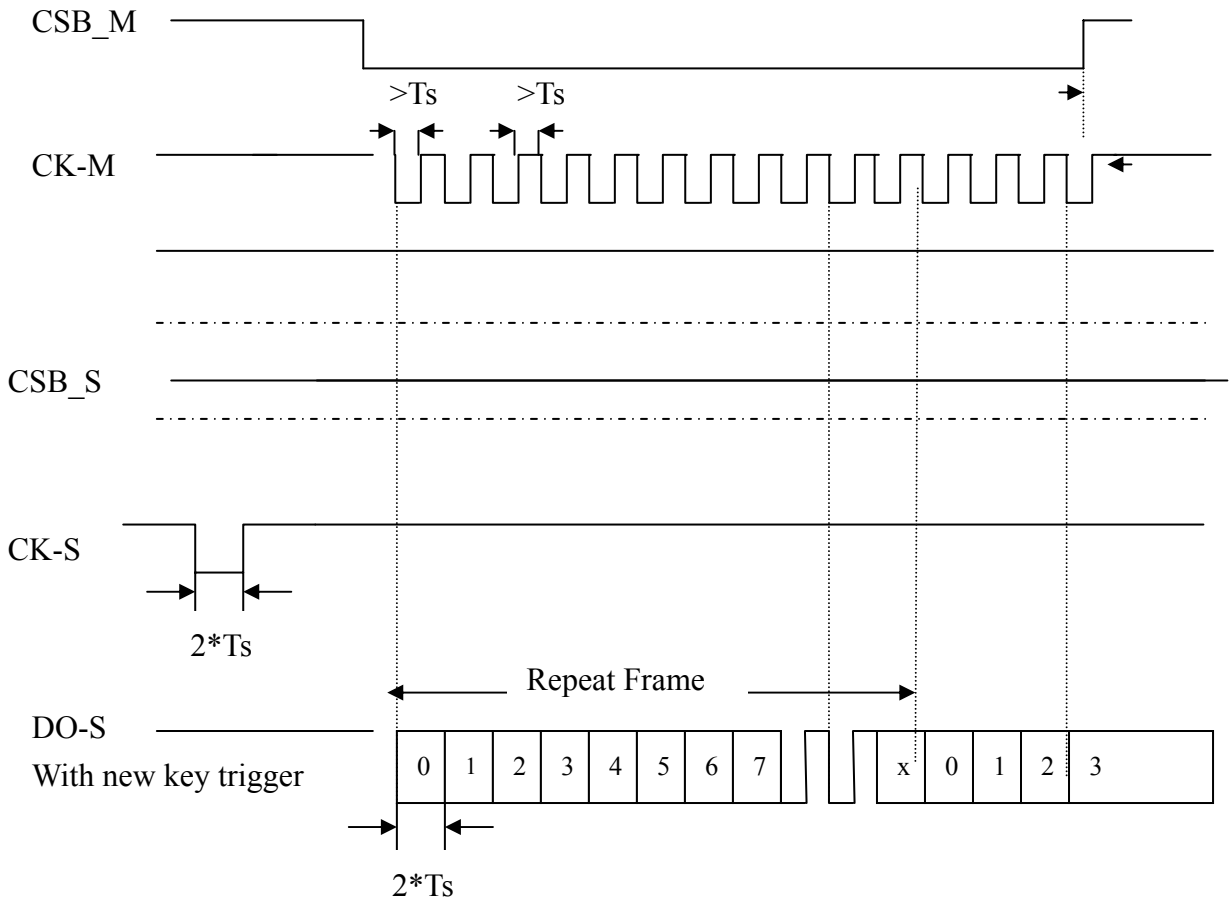
M: Master (User controller)

S: Slave (TTP250)

Ts: The minimum width of level staying time

CSB, CK, DO: Those are open drain with weak pull high resistor IO type

The CSB, CK, DO output waveforms from mater and slave:



Note:

1. Data out sequence is started from I0 and ended at I7. End bit is a sync bit.
2. Master fetches the data at rising edge of CK.
3. DO is synchronized at falling edge of CK.
4. CK-S & CSB-S active as CSB-M=1 for data valid interrupt
5. CSB-M=1 will reset the procedure in initial state.
6. CSB-M ending before clock rising edge
7. x bit default as “1”

2 wires serial interface single mode:

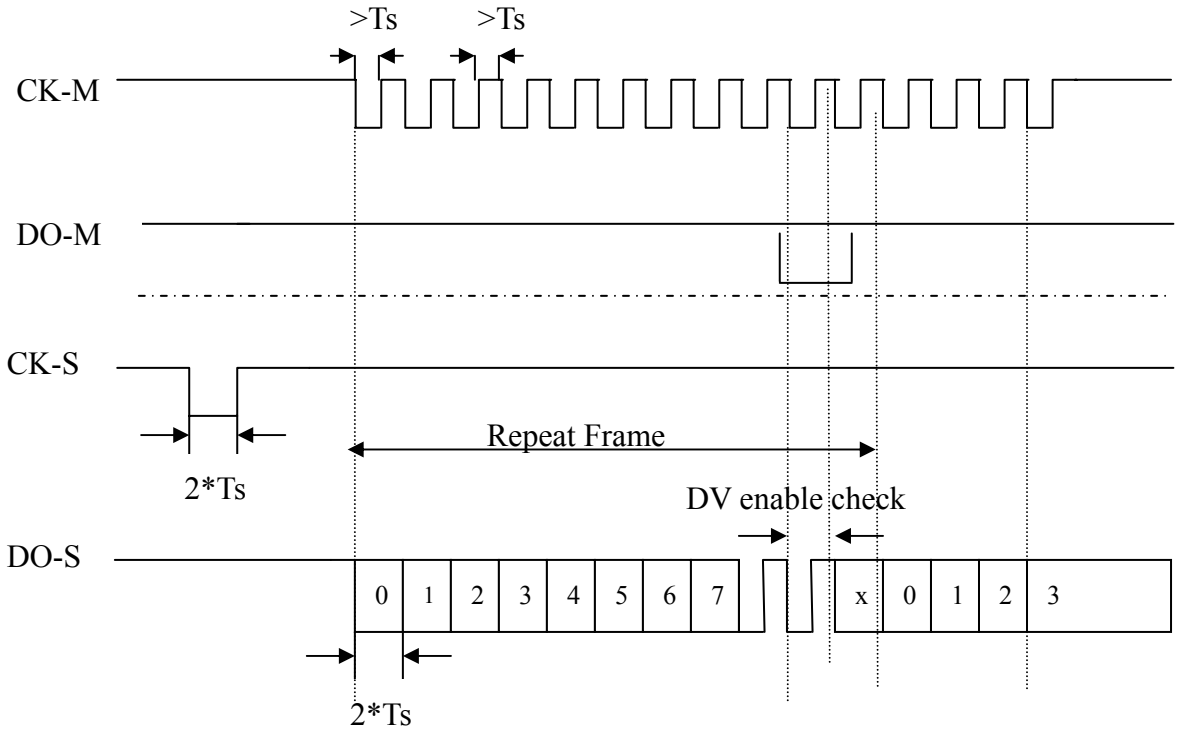
M: Master (User controller)

S: Slave (TTP250)

Ts: The minimum width of level staying time

CK, DO : Those are open drain with weak pull high resistor IO type

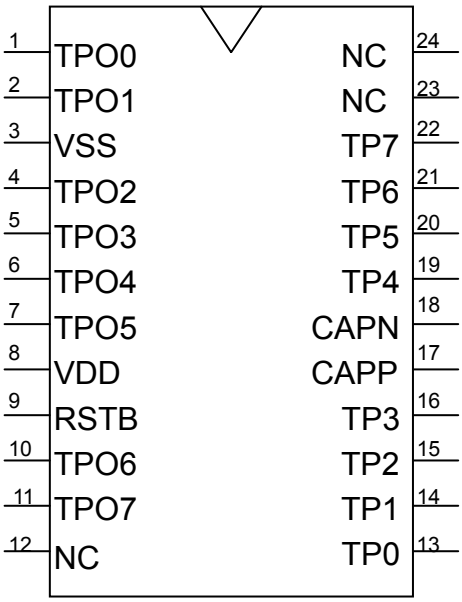
The CK, DO output waveforms from mater and slave:



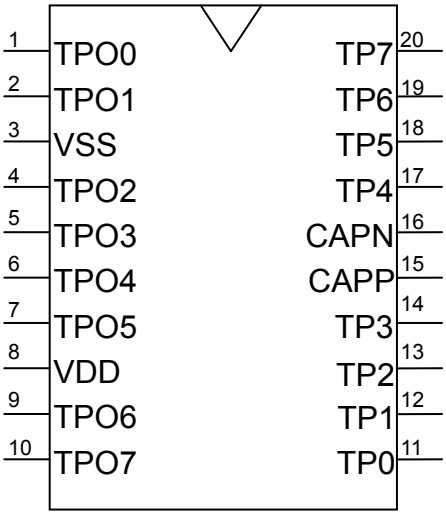
Note:

1. Data out sequence is started from I0 and ended at I7. End bit is a sync bit.
2. Master fetches the data at rising edge of CK.
3. DO is synchronized at falling edge of CK.
4. CK-S can reactive after DO-M stuck zero at DV enable check for data valid interrupt, Do-M low masking width should cover whole check period.
5. x bit default as “1”

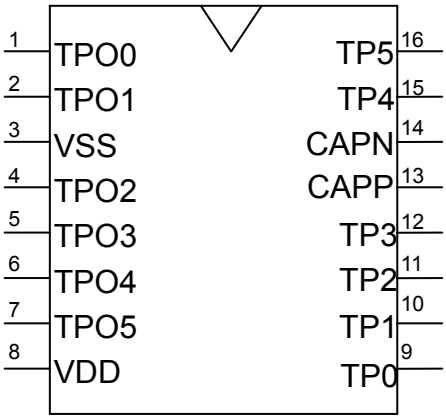
5. Pin Assignment



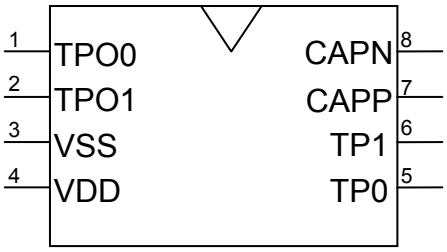
SKINNY DIP/SOP/SSOP - 24PIN



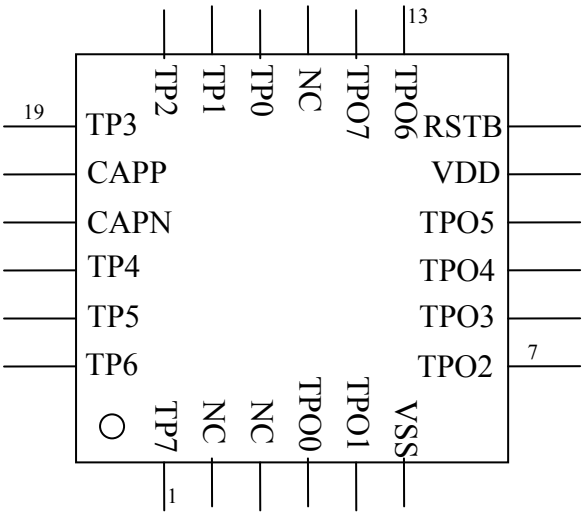
DIP/SOP/SSOP/TSSOP - 20PIN



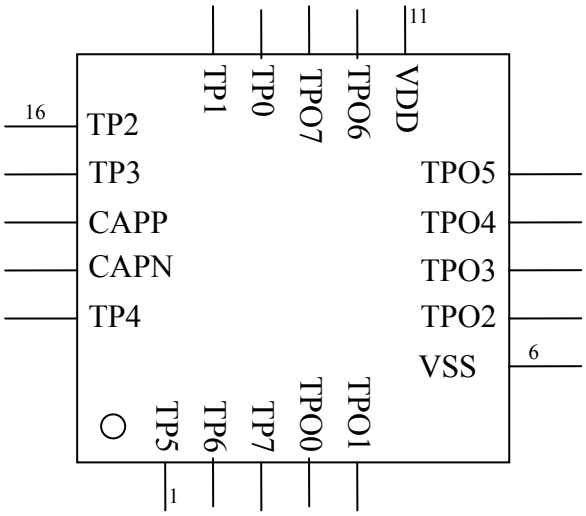
DIP/SOP/SSOP - 16PIN



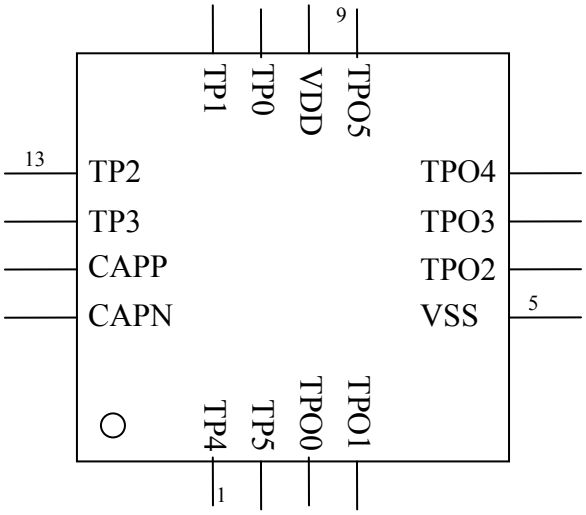
DIP/SOP - 8PIN



QFN-24 PIN



QFN-20 PIN



QFN-16 PIN

6. Pin description

SKINNY DIP/SOP/SSOP - 24PIN				
Pin No.	Pin Name	Type	Function Description	Note
1	TPO0	I/O	TP0 output pin	
2	TPO1	I/O	TP1 output pin	
3	VSS	P	Ground	
4	TPO2	I/O	TP2 output pin	
5	TPO3	I/O	TP3 output pin	
6	TPO4	I/O	TP4 output pin	
7	TPO5	I/O	TP5 output pin	
8	VDD	P	Power	
9	RESB	I	Reset Pin	
10	TPO6	I/O	TP6 output pin	
11	TPO7	I/O	TP7 output pin	
13	TP0	I	Sense Pin	
14	TP1	I	Sense Pin	
15	TP2	I	Sense Pin	
16	TP3	I	Sense Pin	
17	CAPP	I	Connect to Cs	
18	CAPN	O	Connect to Cs	
19	TP4	I	Sense Pin	
20	TP4	I	Sense Pin	
21	TP5	I	Sense Pin	
22	TP7	I	Sense Pin	

DIP/SOP/SSOP/TSSOP - 20PIN				
Pin No.	Pin Name	Type	Function Description	Note
1	TPO0	I/O	TP0 output pin	
2	TPO1	I/O	TP1 output pin	
3	VSS	P	Ground	
4	TPO2	I/O	TP2 output pin	
5	TPO3	I/O	TP3 output pin	
6	TPO4	I/O	TP4 output pin	
7	TPO5	I/O	TP5 output pin	
8	VDD	P	Power	

9	TPO6	I/O	TP6 output pin	
10	TPO7	I/O	TP7 output pin	
11	TP0	I	Sense Pin	
12	TP1	I	Sense Pin	
13	TP2	I	Sense Pin	
14	TP3	I	Sense Pin	
15	CAPP	I	Connect to Cs	
16	CAPN	O	Connect to Cs	
17	TP4	I	Sense Pin	
18	TP4	I	Sense Pin	
19	TP5	I	Sense Pin	
20	TP7	I	Sense Pin	

DIP/SOP/SSOP - 16PIN				
Pin No.	Pin Name	Type	Function Description	Note
1	TPO0	I/O	TP0 output pin	
2	TPO1	I/O	TP1 output pin	
3	VSS	P	Ground	
4	TPO2	I/O	TP2 output pin	
5	TPO3	I/O	TP3 output pin	
6	TPO4	I/O	TP4 output pin	
7	TPO5	I/O	TP5 output pin	
8	VDD	P	Power	
9	TP0	I	Sense Pin	
10	TP1	I	Sense Pin	
11	TP2	I	Sense Pin	
12	TP3	I	Sense Pin	
13	CAPP	I	Connect to Cs	
14	CAPN	O	Connect to Cs	
15	TP4	I	Sense Pin	
16	TP4	I	Sense Pin	

DIP/SOP - 8PIN				
Pin No.	Pin Name	Type	Function Description	Note
1	TPO0	I/O	TP0 output pin	
2	TPO1	I/O	TP1 output pin	
3	VSS	P	Ground	
4	VDD	P	Power	
5	TP0	I	Sense Pin	
6	TP1	I	Sense Pin	
7	CAPP	I	Connect to Cs	
8	CAPN	O	Connect to Cs	

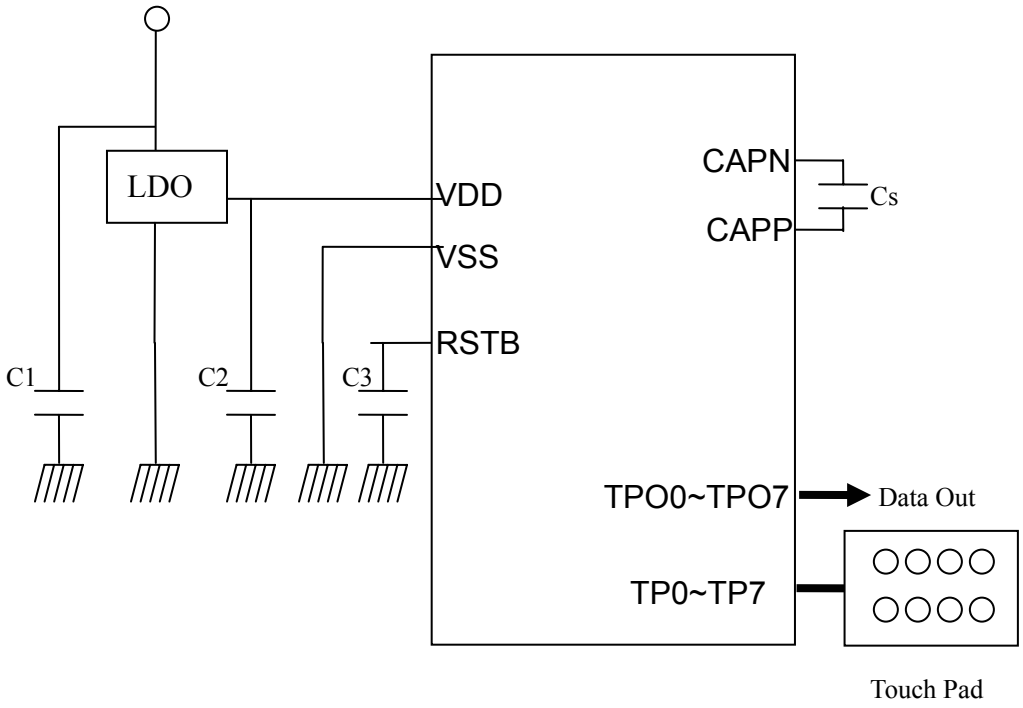
QFN - 24PIN				
Pin No.	Pin Name	Type	Function Description	Note
4	TPO0	I/O	TP0 output pin	
5	TPO1	I/O	TP1 output pin	
6	VSS	P	Ground	
7	TPO2	I/O	TP2 output pin	
8	TPO3	I/O	TP3 output pin	
9	TPO4	I/O	TP4 output pin	
10	TPO5	I/O	TP5 output pin	
11	VDD	P	Power	
12	RESB	I	Reset Pin	
13	TPO6	I/O	TP6 output pin	
14	TPO7	I/O	TP7 output pin	
16	TP0	I	Sense Pin	
17	TP1	I	Sense Pin	
18	TP2	I	Sense Pin	
19	TP3	I	Sense Pin	
20	CAPP	I	Connect to Cs	
21	CAPN	O	Connect to Cs	
22	TP4	I	Sense Pin	
23	TP4	I	Sense Pin	
24	TP5	I	Sense Pin	
1	TP7	I	Sense Pin	

QFN - 20PIN				
Pin No.	Pin Name	Type	Function Description	Note
4	TPO0	I/O	TP0 output pin	
5	TPO1	I/O	TP1 output pin	
6	VSS	P	Ground	
7	TPO2	I/O	TP2 output pin	
8	TPO3	I/O	TP3 output pin	
9	TPO4	I/O	TP4 output pin	
10	TPO5	I/O	TP5 output pin	
11	VDD	P	Power	
12	TPO6	I/O	TP6 output pin	
13	TPO7	I/O	TP7 output pin	
14	TP0	I	Sense Pin	
15	TP1	I	Sense Pin	
16	TP2	I	Sense Pin	
17	TP3	I	Sense Pin	
18	CAPP	I	Connect to Cs	
19	CAPN	O	Connect to Cs	
20	TP4	I	Sense Pin	
1	TP4	I	Sense Pin	
2	TP5	I	Sense Pin	
3	TP7	I	Sense Pin	

QFN - 16 PIN				
Pin No.	Pin Name	Type	Function Description	Note
3	TPO0	I/O	TP0 output pin	
4	TPO1	I/O	TP1 output pin	
5	VSS	P	Ground	
6	TPO2	I/O	TP2 output pin	
7	TPO3	I/O	TP3 output pin	
8	TPO4	I/O	TP4 output pin	
9	TPO5	I/O	TP5 output pin	
10	VDD	P	Power	
11	TP0	I	Sense Pin	

12	TP1	I	Sense Pin	
13	TP2	I	Sense Pin	
14	TP3	I	Sense Pin	
15	CAPP	I	Connect to Cs	
16	CAPN	O	Connect to Cs	
1	TP4	I	Sense Pin	
2	TP4	I	Sense Pin	

7. Application Circuit



註１. 外接電容(Cs)須使用具溫度穩定性佳的電容如 Mylar 塑膠電容或具溫度補償的 NPO 陶瓷電容，確保按鍵靈敏度不會因環境溫度改變而改變。

註 2. C1 及 C2 請依 LDO 的規格加上所須的電容值。C3 建議使用 104。

8. Electrical Characteristic

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20℃ ~ +70℃	℃
Storage Temperature	Tst	-50℃ ~ +125℃	℃
Supply Voltage	VDD	VSS-0.3 ~VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 to VDD+0.3	V
Human Body Mode	ESD	5	KV
Note: VSS symbolizes for system ground			

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		**2.0**	**-**	5.5	V
Operating Current (Always on)	I_{nd1}	VDD=5.0V, with touch detect, LVR disable	-	2		mA
	I_{nd2}	VDD=3.0V, with touch detect, LVR disable	-	0.9		
Operating Current (Sleep Mode)	I_{sd1}	VDD=5.0V, with touch detect, LVR disable	-		20	uA
	I_{sd2}	VDD=3.0V, with touch detect, LVR disable	-		5	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
RESET & INT	V_{IL}	Input Low Voltage	0	-	0.3	VDD
RESET & INT	V_{IH}	Input High Voltage	0.7	-	1.0	VDD
Output port Sink Current	I_{OL}	VDD=5.0V, V_{OL}=0.6V	-	8	-	mA
Output Port Source Current	I_{OH}	VDD=5V, V_{OH}=VDD-0.7V	-	-4	-	mA
Port A Output port Sink Current	I_{OL}	VDD=5.0V, V_{OL}=0.6V	-	2	-	mA
Port A Output Port Source Current	I_{OH}	VDD=5V, V_{OH}=VDD-0.7V	-	-0.9	-	mA
I/O Port Pull-High Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ
RESET Pull-High Resistor	R_{PH}	VDD=5.0V	30	50	80	KΩ
Low Voltage Reset (LVR)	V_{LVR1}	For AC 5V application	2.4	3.2	4.0	V

§ AC Characteristics:

Parameter	Test Condition	Min	Typ.	Max	Unit
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.	0.1	-	1	s