# DDR2 SDRAM

## MT47H64M4 – 16 Meg x 4 x 4 banks
## MT47H32M8 – 8 Meg x 8 x 4 banks
## MT47H16M16 – 4 Meg x 16 x 4 banks

## Features

- $V_{DD}$ = +1.8V ±0.1V, $V_{DDQ}$ = +1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 4 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 $^{t}$CK
- Selectable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Automotive temperature (AT) option
- RoHS-compliant
- Supports JEDEC clock jitter specification

## Options[1] — Marking

- Configuration
  - 64 Meg x 4 (16 Meg x 4 x 4 banks) — 64M4
  - 32 Meg x 8 (8 Meg x 8 x 4 banks) — 32M8
  - 16 Meg x 16 (4 Meg x 16 x 4 banks) — 16M16
- FBGA package (Pb-free)
  - 60-ball FBGA (8mm x 12mm) x4, x8 — BP
  - 84-ball FBGA (8mm x 14mm) x16 — BG
- FBGA package (lead solder)
  - 60-ball FBGA (8mm x 12mm) x4, x8 — FP
  - 84-ball FBGA (8mm x 14mm) x16 — FG
- Timing – cycle time
  - 3.0ns @ CL = 5 (DDR2-667) — -3
  - 3.75ns @ CL = 4 (DDR2-533) — -37E
  - 5.0ns @ CL = 3 (DDR2-400) — -5E
- Self refresh
  - Standard — None
  - Low-power — L
- Operating temperature
  - Commercial (0°C ≤ $T_C$ ≤ 85°C) — None
  - Industrial (–40°C ≤ $T_C$ ≤ 95°C; –40°C ≤ $T_A$ ≤ 85°C) — IT
  - Automotive (–40°C ≤ $T_C$, $T_A$ ≤ 105°C) — AT
- Revision — :B

Note: 1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.

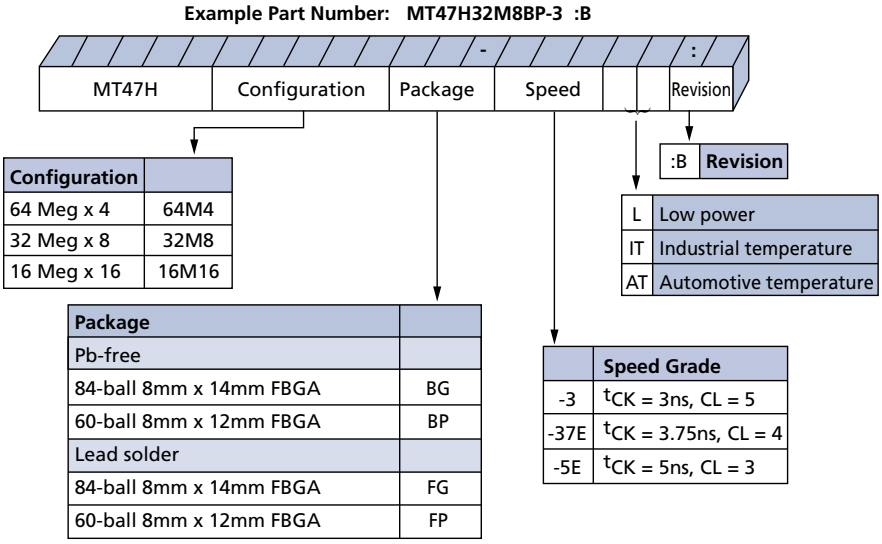
**Table 1: Key Timing Parameters**

| Speed Grade | Data Rate (MT/s) | | | $^{t}$RC (ns) |
|---|---|---|---|---|
| | CL = 3 | CL = 4 | CL = 5 | |
| -3 | 400 | 533 | 667 | 55 |
| -37E | 400 | 533 | n/a | 55 |
| -5E | 400 | 400 | n/a | 55 |

**Table 2: Addressing**

| Parameter | 64 Meg x 4 | 32 Meg x 8 | 16 Meg x 16 |
|---|---|---|---|
| Configuration | 16 Meg x 4 x 4 banks | 8 Meg x 8 x 4 banks | 4 Meg x 16 x 4 banks |
| Refresh count | 8K | 8K | 8K |
| Row address | A[12:0] (8K) | A[12:0] (8K) | A[12:0] (8K) |
| Bank address | BA[1:0] (4) | BA[1:0] (4) | BA[1:0] (4) |
| Column address | A[11, 9:0] (2K) | A[9:0] (1K) | A[8:0] (512) |

**Figure 1: 256Mb DDR2 Part Numbers**




Note: 1. Not all speeds and configurations are available in all packages.

## FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

# Ball Assignments and Descriptions

**Figure 6: 60-Ball FBGA – x4, x8 Ball Assignments (Top View)**

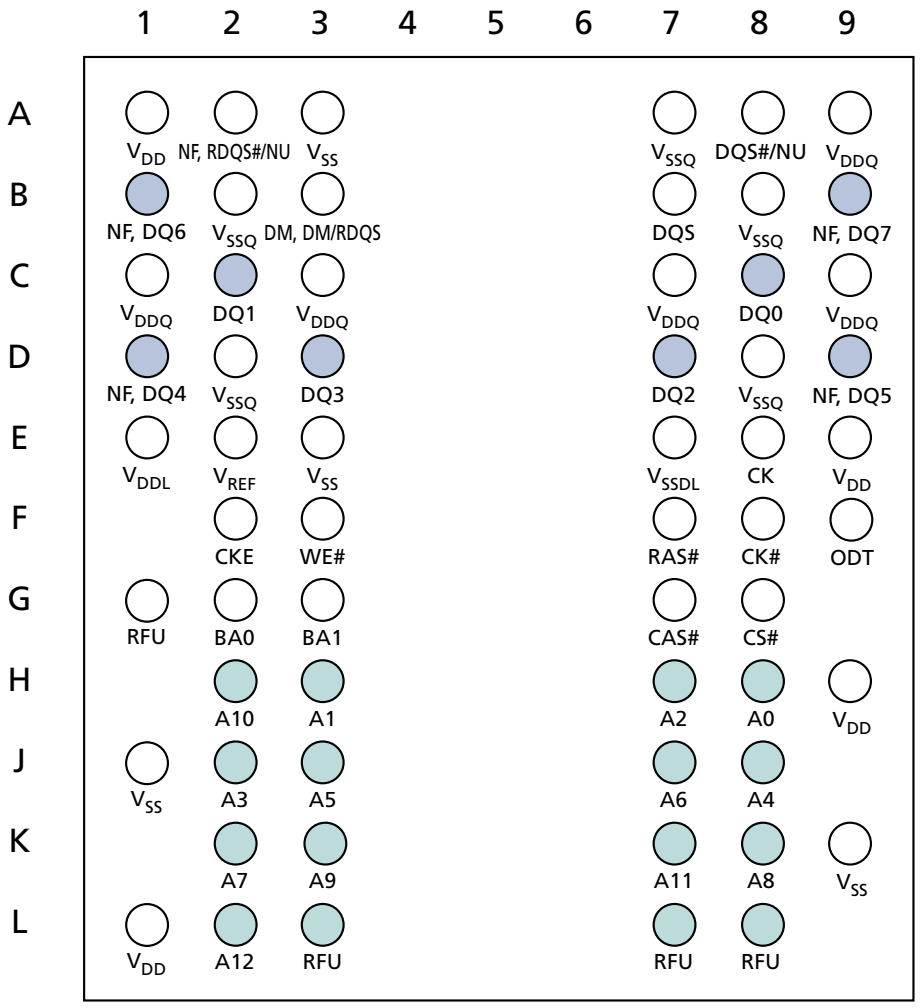
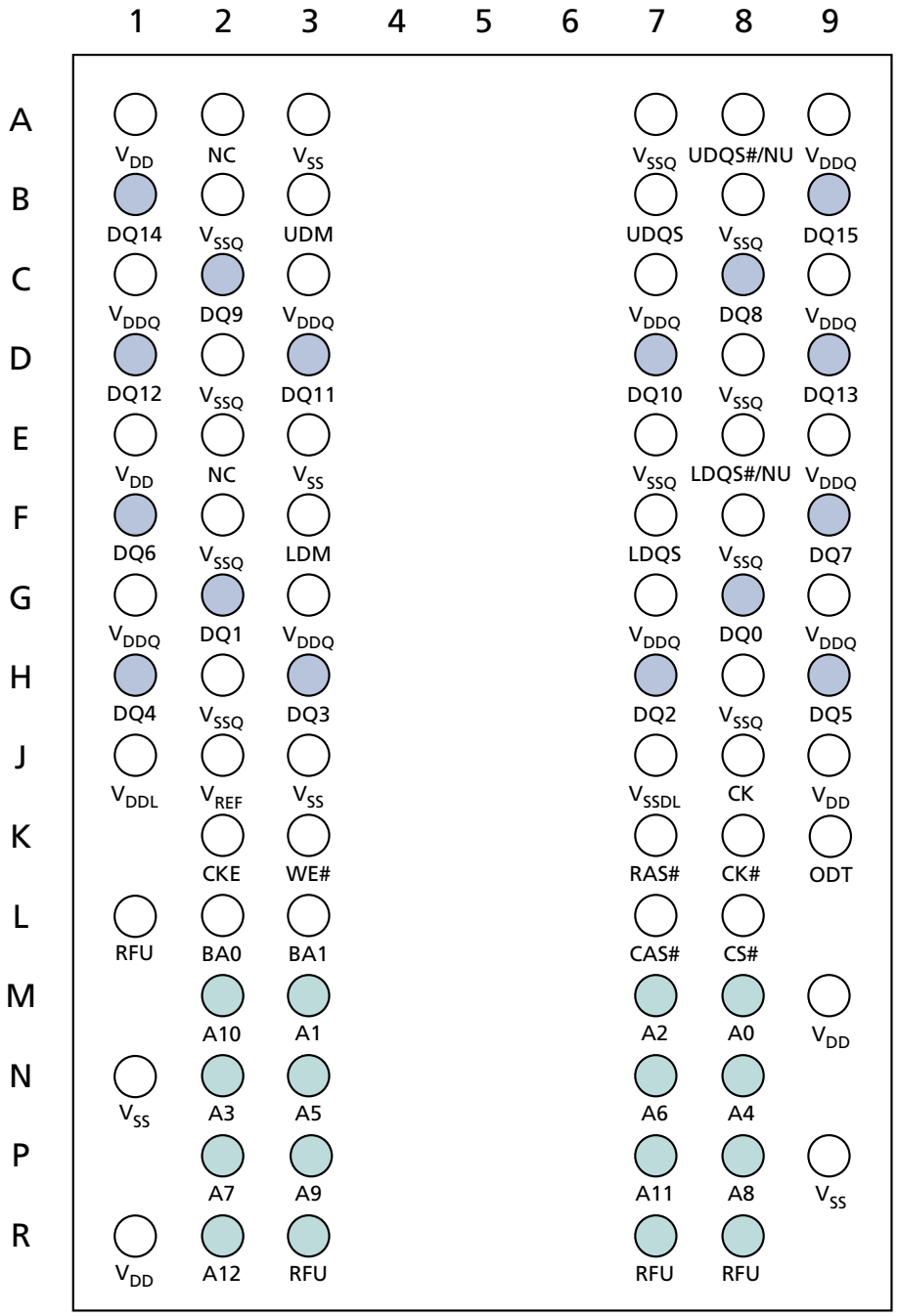


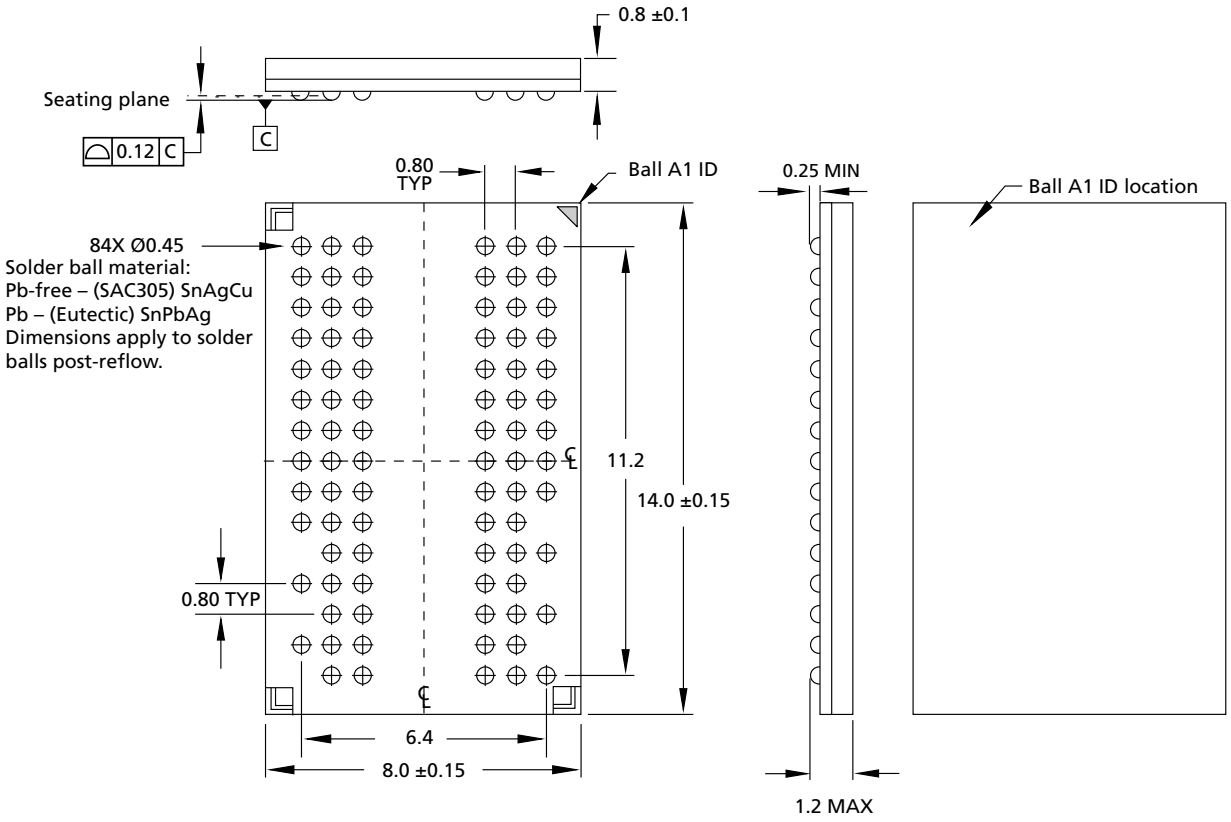
**Figure 7: 84-Ball FBGA – x16 Ball Assignments (Top View)**



# Packaging

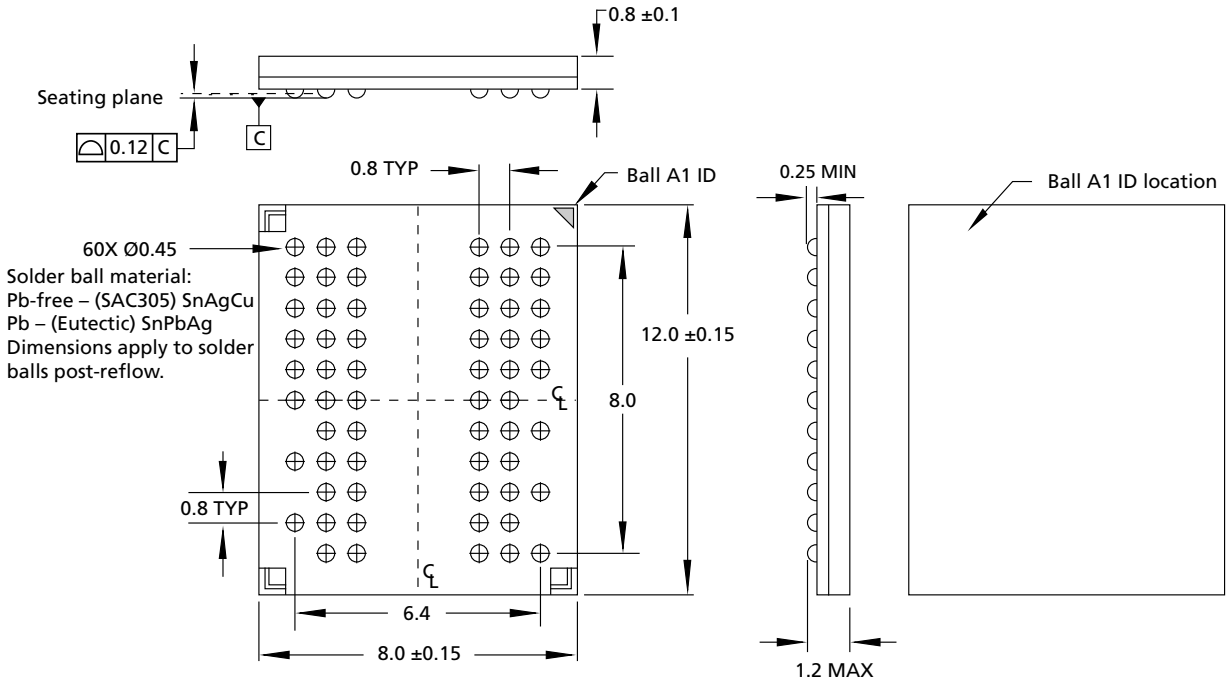
## Package Dimensions

**Figure 8: 84-Ball, FBGA Package (8mm x 14mm) – x16**




Note: 1. All dimensions are in millimeters.

**Figure 9: 60-Ball, FBGA Package (8mm x 12mm) – x4, x8**




Note: 1. All dimensions are in millimeters.