

Parameters Subject to Change Without Notice

DESCRIPTION

JW7707D is a synchronous rectifier for Flyback converters. It integrates a 60V power MOSFET that can replace Schottky diode for high efficiency. It turns on the internal MOSFET if the $V_{SW} < -500\text{mV}$ and turns it off before the current from GND to SW is lower than zero.

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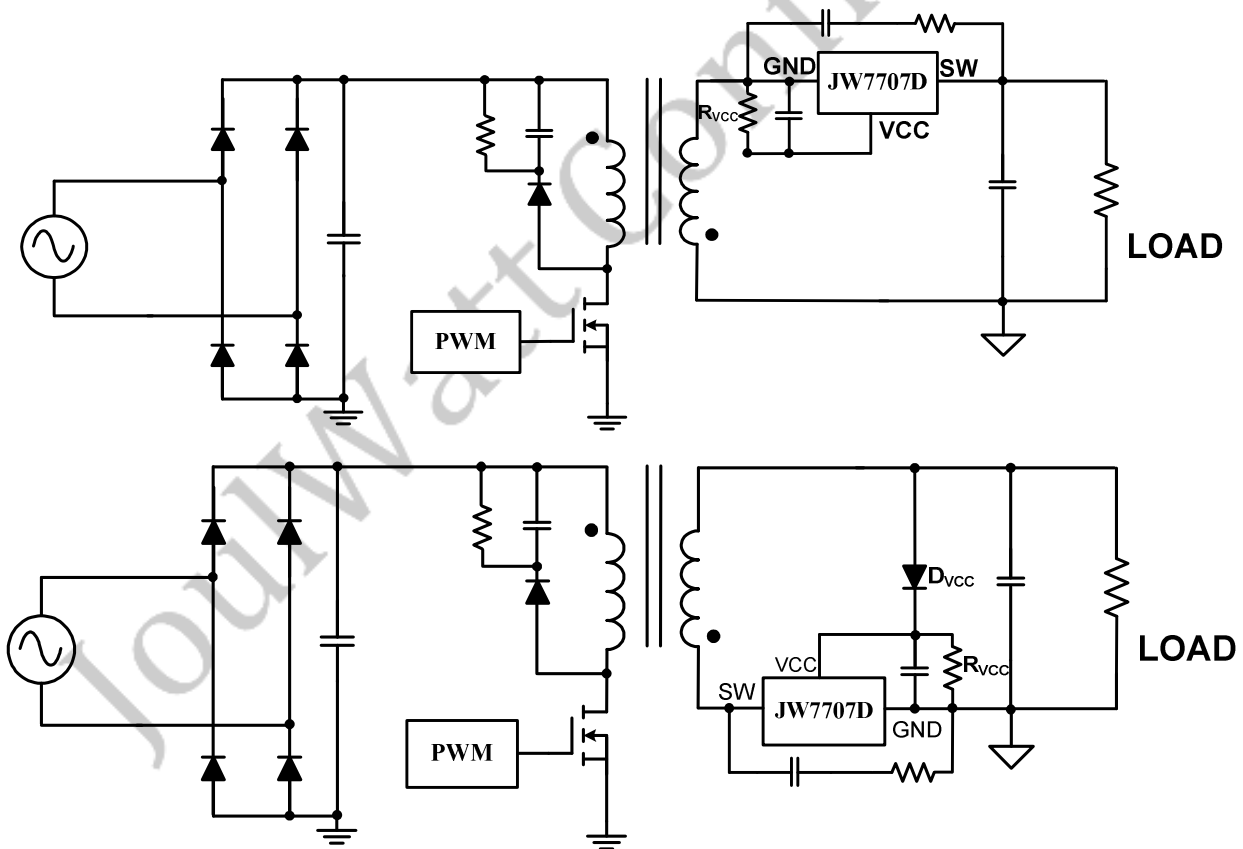
FEATURES

- Supports DCM and Quasi-Resonant Flyback converter
- Integrated 10mΩ 60V Power MOSFET
- Supports High-side and Low-side Rectification
- No need external power supply

APPLICATIONS

- Flyback converters
- Adaptors

TYPICAL APPLICATION



Note 1: R_{VCC} is recommended in case IC is damaged in CCM.

Note 2: D_{VCC} is recommended if VCC voltage is too low in light load.

ORDER INFORMATION

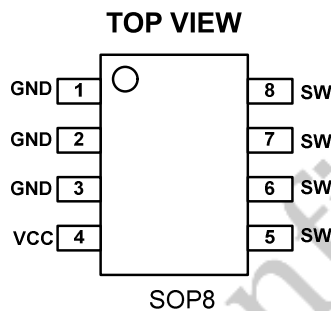
LEAD FREE FINISH	TAPE AND REEL ¹⁾	BULK	TRAY	PACKAGE	TOP MARKING ²⁾
JW7707DSOPB#PBF	JW7707DSOPB#TRPBF	-	-	SOP8	JW7707D XXXXXXX

Notes:

- JW #TRPBF

PB Free
 Tape and Reel (If "TR" is not shown, it means tube)
 Part No. Package Code
- Line 1 of top marking means Part No., and the line 2 of top marking means Date Code.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

SW PIN	65V
VCC PIN	24V
Maximum Power Dissipation ²⁾	2.5W
Junction Temperature ³⁾	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to 150°C

RECOMMENDED OPERATING CONDITIONS

SW Pin	20V to 55V
VCC PIN	7V to 9V
Operation Junction Temp.	-40°C to 125°C

THERMAL PERFORMANCE⁴⁾

	θ_{JA}	θ_{JC}
SOP8	96	45°C/W

Note:

- Exceeding these ratings may damage the device.
- TA=25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

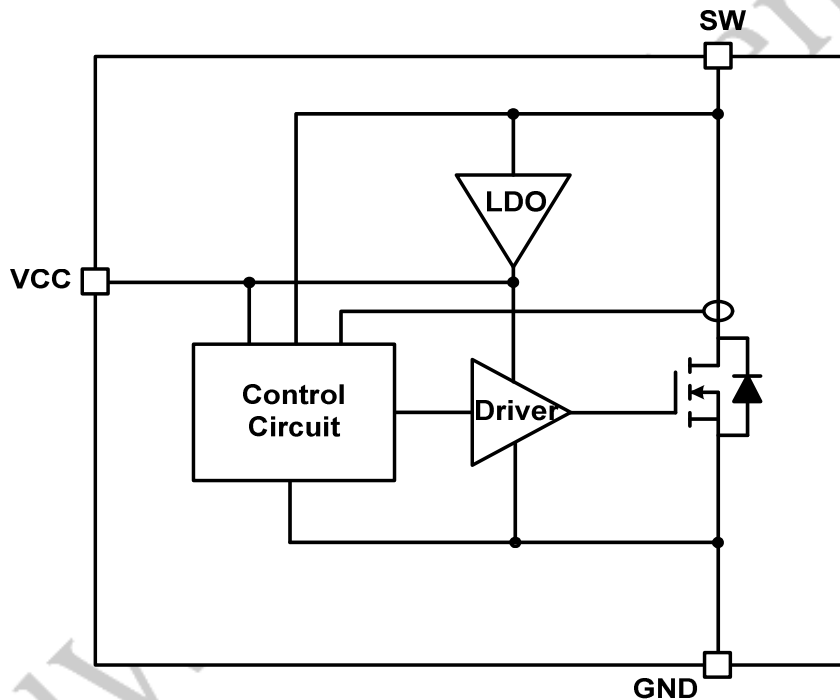
$T_A = 25^\circ\text{C}$, unless otherwise stated.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
VCC Section						
VCC Operation Voltage	V_{CC}	SW=40V, VCC=0.1uF	7.4	7.75	8.1	V
VCC Start up Voltage	$V_{CC_STAR\ UP}$		3.6	3.8	4	V
VCC UVLO	V_{CC_UVLO}		3.5	3.65	3.8	V
Quiescent Current	I_Q	VCC=6.5V, C _{vcc} =0.1uF	70	85	100	uA
Internal MOS Section						
Internal MOS R _{dson}	R _{dson}	VCC=8.5V, I _{sw} =10A		10	15	mΩ
Maximum Peak Current	I _{peak}	T _J =25°C		75		A
Drain Current-continuous	I _D	T _J =25°C		30		A
Internal MOS turn on delay	T _{DON}			24		nS
Internal MOS turn off delay	T _{DOFF}			10		nS
Internal MOS turn on minimum time	T _{ON_MIN}			1		uS
Internal MOS turn off minimum time	T _{OFF_MIN}		2.5	3.5		uS
SW Section						
Internal MOS turn on Threshold	V _{MOS_ON}			-0.5		V
SW to GND Breakdown Voltage	V _{(BR)DSS}	VCC=9V, I _{sw} =250uA	60			V

PIN DESCRIPTION

Pin No.	Name	Description
1、2、3	GND	Ground
4	VCC	Power supply, Bypass a capacitor between VCC and GND.
5、6、7、8	SW	Internal Power MOSFET Drain.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

JW7707D is a synchronous rectifier, it can replace the Schottky to improve the efficiency in Flyback converters. It supports operation in DCM and Quasi-Resonant Flyback converters. It can power itself through the internal LDO during the turn-off period, a 0.1uF capacitor is needed between VCC and GND.

Turn-on Blanking Time

The control circuitry contains a blanking function. When the internal MOSFET is turned on, it at least last for some time, the turn on blanking time is about 1uS. During the turn on blanking period, the turn off threshold is not totally blanked, but changes the threshold current. This assures that the internal MOSFET can always be turned off even during the blanking period.

Under-Voltage Lockout (UVLO)

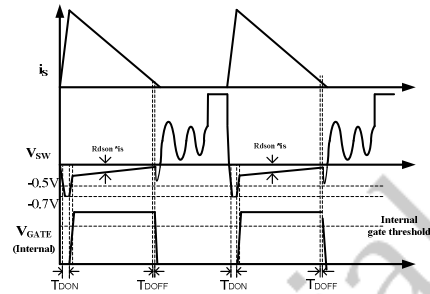
When the VCC is below UVLO threshold, the internal MOSFET is turned off and never turned on before the VCC exceeds the startup voltage.

Turn On Phase

The switch current first flows through the body diode of integrate MOSFET, which generates a negative V_{SW} . When the V_{SW} is higher than 0.7V and then V_{SW} is lower than V_{MOS_ON} , it turns on the integrate MOSFET after 24ns delay.

Turn Off Phase

The JW7707D senses the current of the internal MOSFET I_{SW} , before I_{SW} is lower than Internal MOS turn off threshold, the driver voltage of the switch is pulled down to zero after 10ns delay.



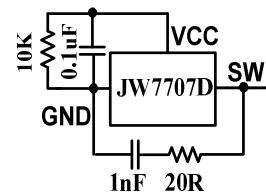
Turn on and turn off delay

Startup

During the startup period, when the VCC is lower than startup voltage, the internal MOSFET is turned off. The current flows through body diode until the VCC exceeds the startup voltage.

RC Snubber Circuit

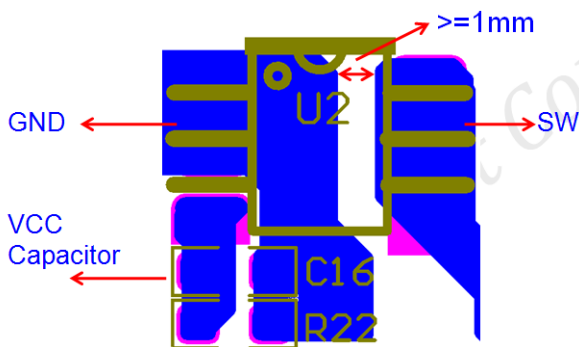
In some applications (output short circuit protection), the inductor current may go into slight CCM condition. To avoid the voltage spike across the synchronous rectifier, we suggest RC snubber should be placed between SW and GND, and a resistor should be paralleled with VCC capacitor.



RC Snubber circuit

PCB Layout Guidelines

1. The VCC pin must be locally bypassed with a capacitor.
2. The PAD must be connected to main power loop.
3. The distance between GND and SW should be more than 1mm in case of too much couple noise.
4. The EUT, a 5V/2A adaptor⁴⁾, can pass $\pm 25KV$ air discharging test by following with the recommended layout .



The recommended layout

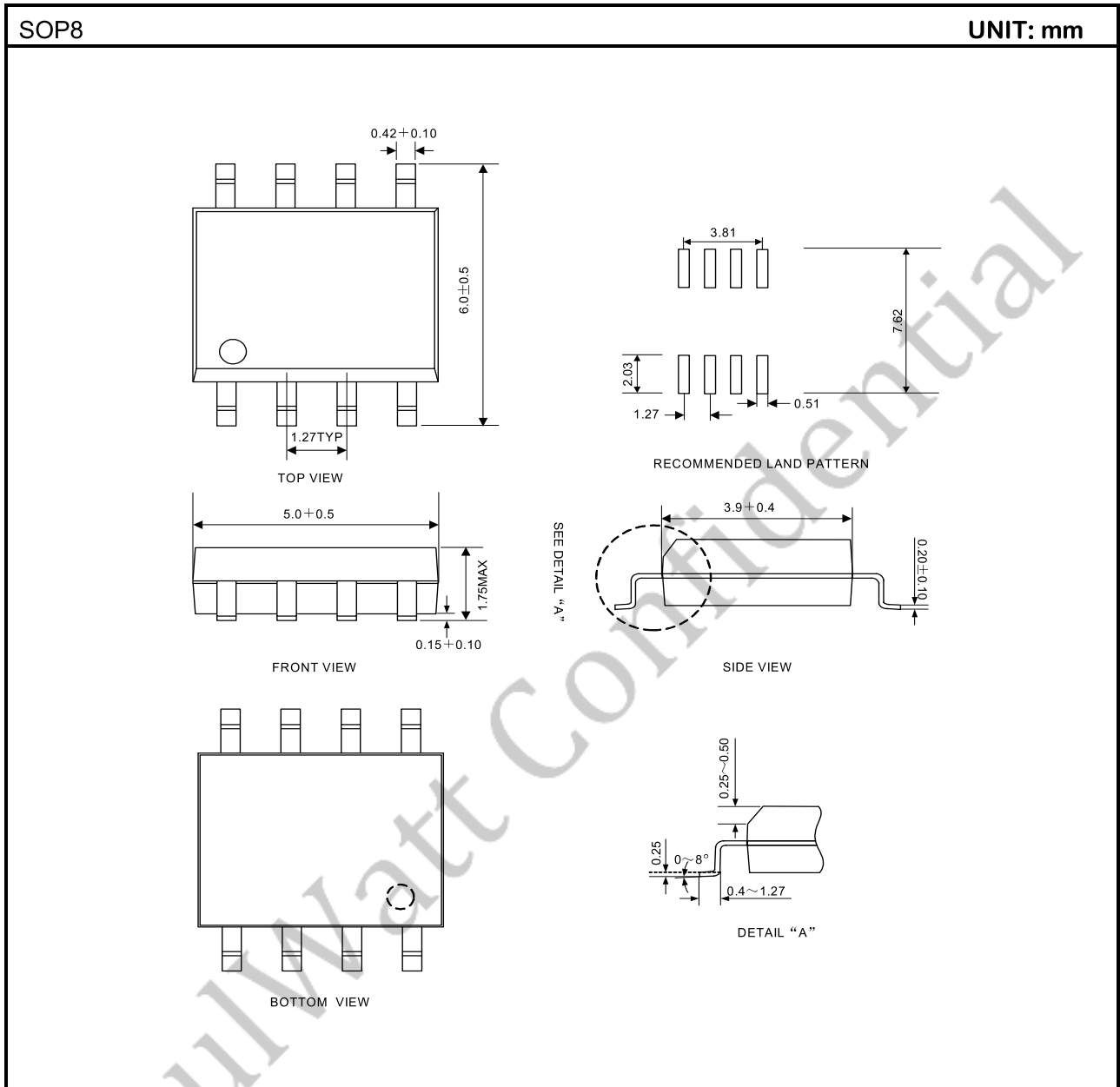
1. JW7707D is Moisture-Sensitive Devices and its MSL⁵⁾ (Moisture-Sensitive Level) is level-3.
2. Calculated shelf life in sealed bag is 12 months at $<40^{\circ}C$ and $<90\%RH$ (Relative Humidity).
3. Peak package body temperature⁵⁾ is $260^{\circ}C$.
4. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
 - a) Mounted within 168 hours of factory at the condition $\leq 30^{\circ}C/60\%RH$.
 - b) Stored at $<10\%RH$.
5. Devices require bake before mounting if Humidity Indicator Car(HIC) is $>10\%RH$ when read at $23 \pm 5^{\circ}C$.
6. If baking is required, devices may be baked for 48 hours at $125 \pm 5^{\circ}C$. If device containers cannot be subjected to high temperature for shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure.

Package and Bag Caution

Note:

- 4) ESD pass criterion is $\pm 15KV$ air discharging according to IEC61000-4-2. And the test equipment is TESEQ NSG 438.
- 5) Level and body temperature defined by IPC/JEDEC J-STD-020.

PACKAGE OUTLINE



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