JW5510

20V 10A Fully-integrated Synchronous Boost Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®5510 is a highly integrated Boost converter and can be widely used in portable applications.

The JW5510 implements a synchronous high-efficiency step-up boost converter with 10A switch current capability and is capable of providing an output voltage up to 20V.

The integrated low Rds(on) MOSFET minimizes physical footprint, maximizes the efficiency, which reduces the power dissipation. Constant current control is utilized to protect the device from overshooting in unwanted conditions. Built-in loop compensation simplifies the circuit and design. PFM is engaged to maintain high efficiency at light load.

JW5510 guarantees robustness with thermal protection and under voltage lockout.

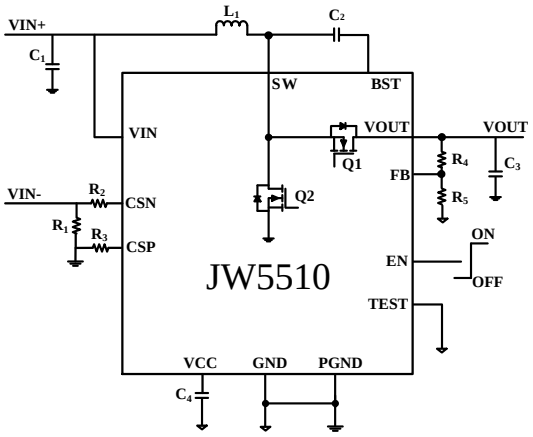
FEATURES

- 3.0V to 20V Input Voltage Range
- 4.0V to 20V Output Voltage Range
- Integrate Low R_{DSON} Switch Power MOS and Synchronous Rectifier MOS.
- 10A Switch Current Limit
- Switch Frequency: 400kHz.
- High Efficiency over Full Load Range
- Thermal Shutdown
- QFN3*4 Package

APPLICATIONS

- Battery Powered system
- Electronic Cigarette
- Bluetooth Speaker

TYPICAL APPLICATION

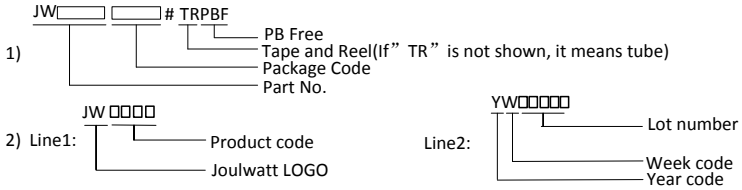


Typical application circuit

ORDER INFORMATION

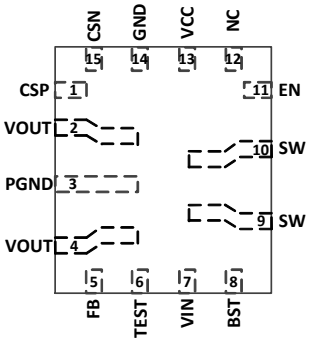
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW5510QFNE#TRPBF	QFN3×4-15	JW5510 YW□□□□□

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, VOUT, SW, FB Pin .....-0.3V to 25V
BST-SW .....-0.3V to 6.5V
All Other Pins .....-0.3V to 6.5V
JunctionTemperature[2)3)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS

Output Voltage VOUT .....4.0V to 20V
Input Voltage VIN .....3.0V to 20V
Operation Junction Temp (T_J) .....-40ºC to +125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{JC}
QFN3X4-15	48	11ºC/W

Note：

1) Exceeding these ratings may damage the device.

2) The JW5510 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) The JW5510 includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN=5V, TA=25℃, unless otherwise stated

Item	Symbol	Condition	Min.	Typ.	Max.	Units
General parameters						
VIN Voltage Range	V_{IN}		3.0		20	V
VOUT voltage Range	V_{OUT}		4.0		20	V
VCC output voltage	V_{CC}	I_{VCC}=2mA		4.9		V
VCC output current limit	I_{VCC}	VCC>2.7V		50		mA
Supply current in shut-down mode	I_Q	V_{IN}=4V, EN=0V		65		μA
Switch frequency	F_{sw}			400		kHz
Switch minimum off time	T_{off_min}		80	100	120	ns
EN Logic HIGH	V_{ENH}	V_{IN}=8V			2.0	V
EN Logic LOW	V_{ENL}	V_{IN}=8V	0.8			V
Top switch on-resistance	R_{dsbkTG}			12		mΩ
Bottom switch on-resistance	R_{dsbkBG}			12		mΩ
Feedback voltage	V_{FB}			0.9		V
Input average current limit	I_{IN_LIM}	R_1=5mΩ; R_2=R_3=3kΩ;		6		A
Protection						
VOUT OVP threshold	V_{O_OVP}	VOUT rising		23.2		V
		VOUT falling		21.5		V
VOUT OVP deglitch time	t_{O_OVP}			2		μs
VIN UVLO threshold	V_{IN_UVLO}	VIN rising		3.0		V
		VIN falling		2.7		V
Thermal shutdown threshold[5)]	T_{SHUT}			150		°C
Thermal recovery threshold[5)]	T_{REC}			130		°C

Notes:

5) Guaranteed by design.

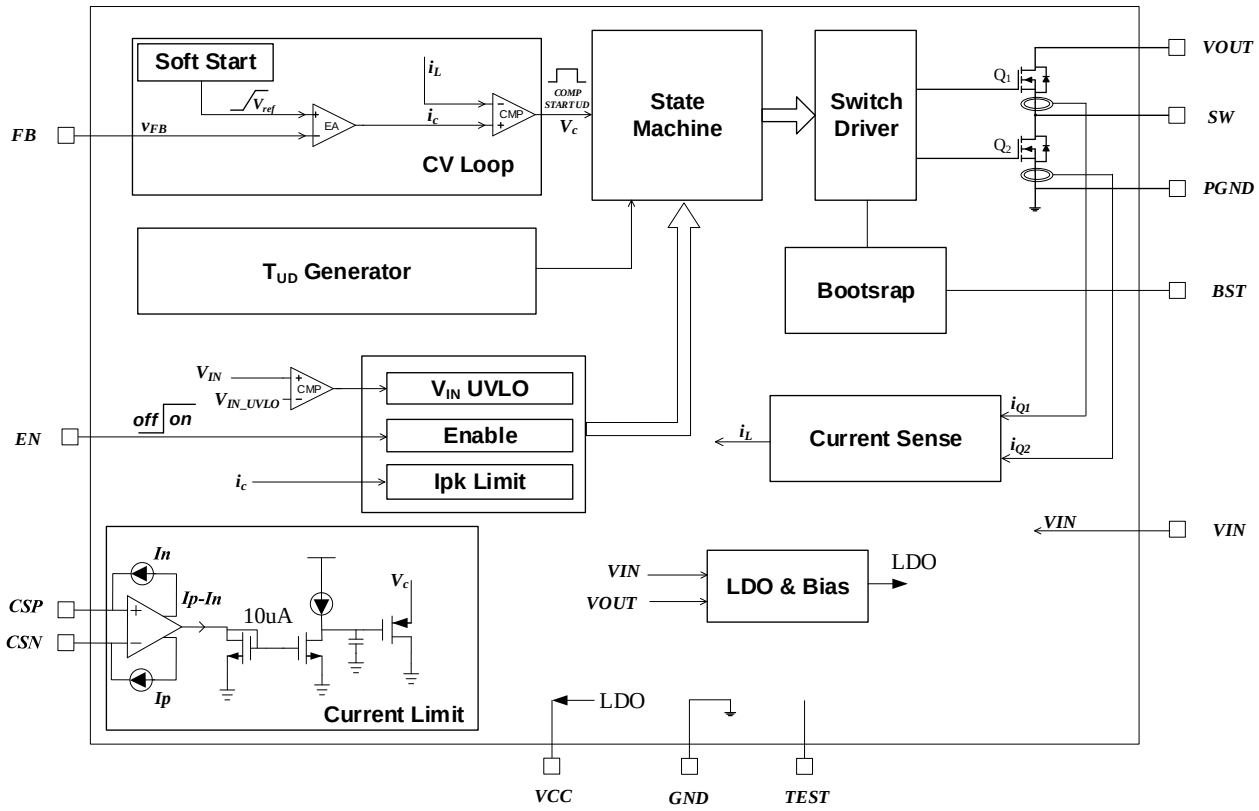
PIN DESCRIPTION

Pin No.	Name	Description
1	CSP	Positive terminal of current sense.
2, 4	**VOUT**	**Output pin, connect this pin to GND with ceramic capacitor.**
3	**PGND**	**Power Ground.**
5	FB	Output feedback pin.
6	TEST	Test pin. Tie this pin to GND for normal operation. Do not allow this pin to float.
7	VIN	Input voltage sense pin.
8	BST	Bootstrap supply pin for top switch. Connect this pin to SW with a 0.1μF capacitor.
9, 10	**SW**	**Power switching node. Connect to input with inductor**
11	EN	Enable control pin. Forcing the pin below 0.8V shuts down the converter, reducing quiescent current. Once the EN pin rises above 2.0V, the IC is turned on.
12	NC	No connection.
13	VCC	4.9V LDO for power driver and internal circuit. Must be bypassed to GND with a minimum of 10μF ceramic capacitor for stable operation.
14	GND	Signal GND.
15	CSN	Negative terminal of current sense.

Notes:

Highlighted pins are high current pins.

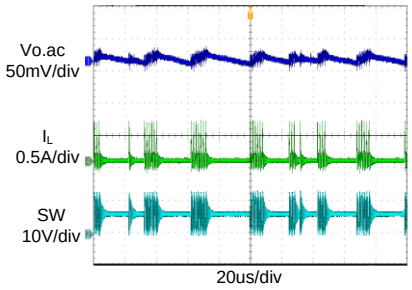
BLOCK DIAGRAM



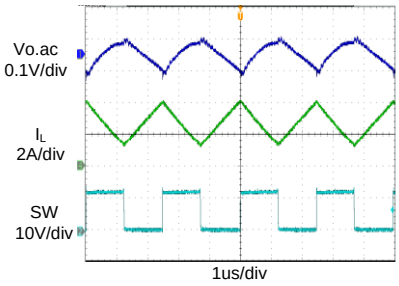
TYPICAL PERFORMANCE CHARACTERISTICS

V_O = 12V, L = 2.4μH, C_{IN} = 22μF×2, C_O=22uF×5, TA = +25°C, unless otherwise noted.

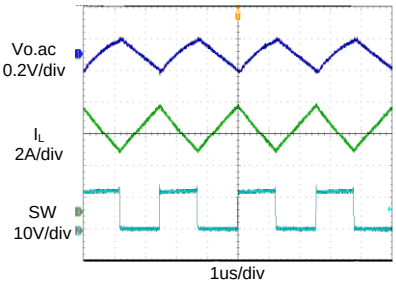
V_{BAT}=6.0V I_O=0.01A



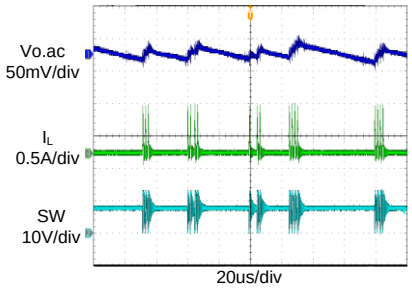
V_{BAT}=6.0V I_O=1.25A



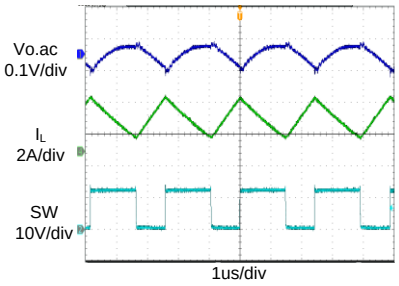
V_{BAT}=6.0V I_O=2.5A



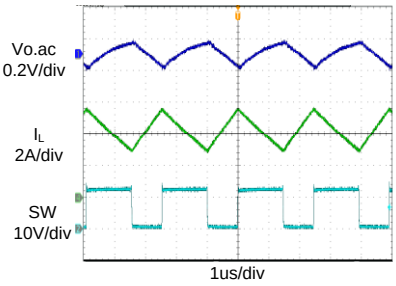
V_{BAT}=7.4V I_O=0.01A



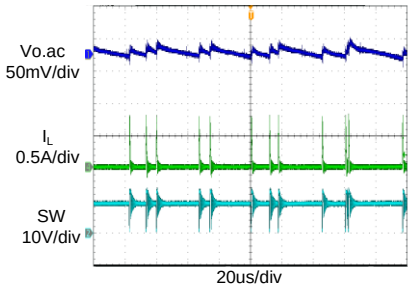
V_{BAT}=7.4V I_O=1.25A



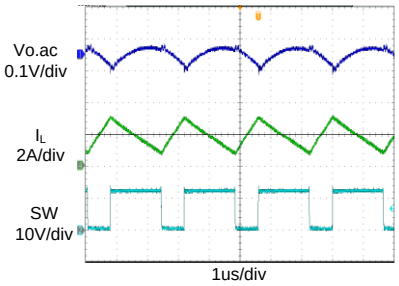
V_{BAT}=7.4V I_O=2.5A



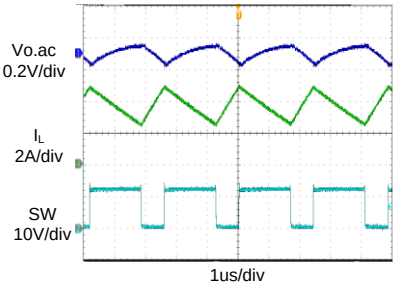
V_{BAT}=8.4V I_O=0.01A



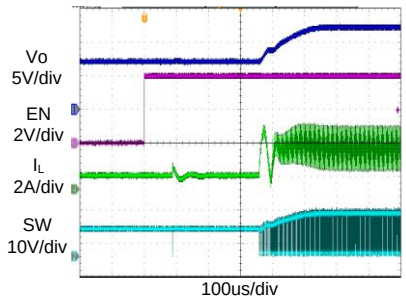
V_{BAT}=8.4V I_O=1.25A



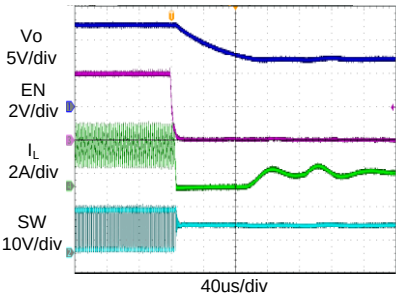
V_{BAT}=8.4V I_O=2.5A



EN ON @ V_{BAT}=7.4V I_O=1.5A

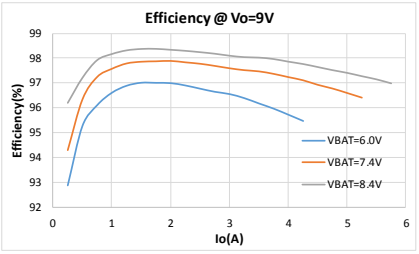


EN OFF @ V_{BAT}=7.4V I_O=1.5A



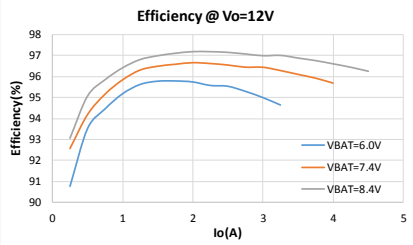
Efficiency vs. Io @ Vo=9V

(2 cells, L=2.4uH)



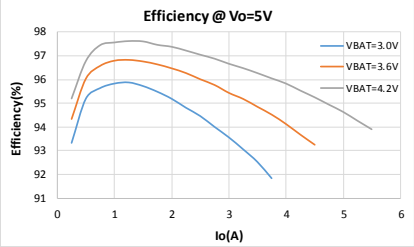
Efficiency vs. Io @ Vo=12V

(2 cells, L=2.4uH)



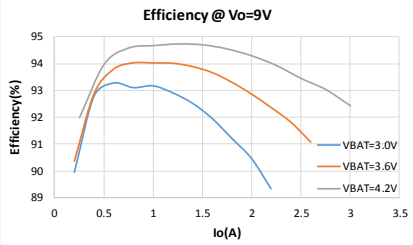
Efficiency vs. Io @ Vo=5V

(single cell, L=1.2uH)



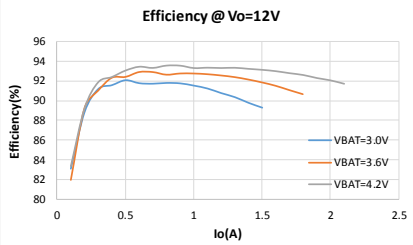
Efficiency vs. Io @ Vo=9V

(single cell, L=1.2uH)



Efficiency vs. Io @ Vo=12V

(single cell, L=1.2uH)



FUNCTIONAL DESCRIPTION

JW5510 is a monolithic DC to DC converter that can operate over a wide input voltage range of 3.0V to 20V. The output voltage can be programmed up to 20V. Internal low R_{DSON} N-channel power switches reduce the solution complexity and increase the efficiency.

Flexible Boost Converter

The JW5510 is a flexible boost DC-DC converter which utilizes proprietary single inductor current-mode control with better dynamic response.

Compensation is done internally on the chip. The JW5510 operates in PFM mode at light load. In PFM mode, switching frequency is continuously controlled in proportion to the load current, i.e. switch frequency is decreased when load current drops to increase power efficiency at light load by reducing switching-loss, minimizing the circuit.

Output voltage

The output voltage is set by an external feedback resistive divider. The feedback signal is compared with internal precision 0.9V voltage reference by an error amplifier. The output voltage is given by the equation:

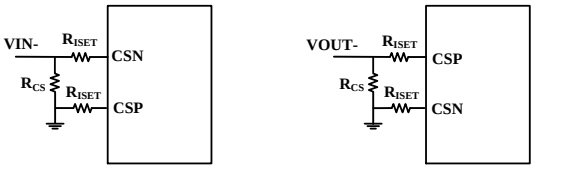
$$V_O(\mathrm{V}) = \frac{0.9(\mathrm{V}) \times (R_4 + R_5)}{R_5}$$

Where R4 and R5 are defined in typical application figure.

Programmable Input / Output Current Limit

As shown in figure1, the current sense resistor R_{CS} should be placed at input terminal or output terminal and closed to the R_{ISET}. The input/output current limit is set by R_{ISET} and R_{CS}, which is optional. If the input/output current limit is not desired, the CSN pin should be shorted to VCC, and the CSP pin shorted to GND.

$$I_{ILIMIT}(\mathrm{A}) = \frac{R_{ISET}(\mathrm{k\Omega})}{R_{CS}(\mathrm{m\Omega})} \times 10(\mu\mathrm{A/A})$$



(a) Input current limit (b) output current limit

Figure 1. Programmable current limit

When the input/output current equals to the current limit threshold, the current limit loop begins to work, it turns down output voltage to limit the output power.

VIN UVLO

When V_{IN} decreases to V_{IN_UVLO}, the converter is terminated. When the V_{IN} recovers and is larger than V_{IN_UVLO}, the JW5510 can re-work if the V_{EN} is still high.

Thermal Control

When the junction temperature of the JW5510 rises above 135°C, it begins to reduce the output power to prevent the temperature from rising further. If the junction temperature of JW5510 rises above 150°C, the chip stops.

Shut-down Mode

The JW5510 shuts down when voltage at EN pin is below 0.8V. The entire regulator is off.

Output Over-Voltage Protection

If the output voltage is larger than V_{O_OVP} rising threshold, the device stops switching. Until the output voltage is less than V_{O_OVP} falling threshold, the device re-starts switching again.

PCB Layout Guidelines

For minimum noise problem and best operating performance, the PCB layout of JW5510 must be carefully designed:

1. The input decoupling capacitor between VIN and GND should be placed as close to the chip as possible for minimum power loop.
2. The output decoupling capacitor between VOUT and GND should be arranged between the two VOUT pins symmetrically.

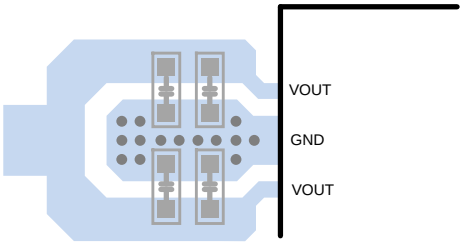


Figure 2. Layout of output capacitors

3. The current sense resistor should be connected to the CSP, CSN pins through R_{ISET} resistors in Kelvin sense way for better current accuracy, as shown in the figure below

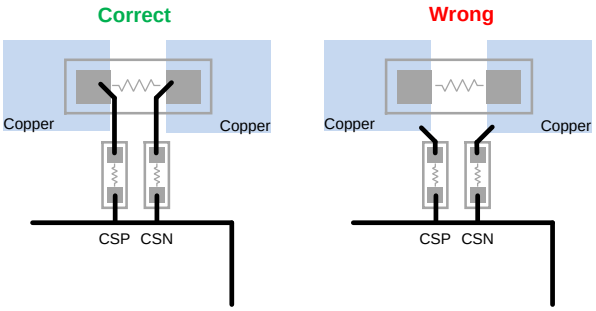


Figure 3. Layout of current sense resistor

4. The ground copper on the PCB should be as large as possible for better heat performance.

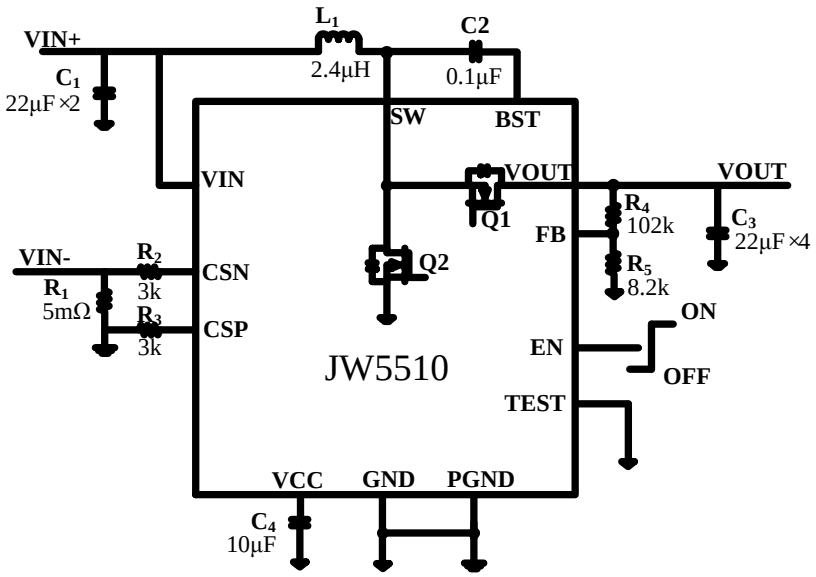
REFERENCE DESIGN

Reference 1：Input current limit set

V_{IN}: 6.0V ~ 8.4V

V_{OUT}: 12V

I_{IN_LIM}: 6A



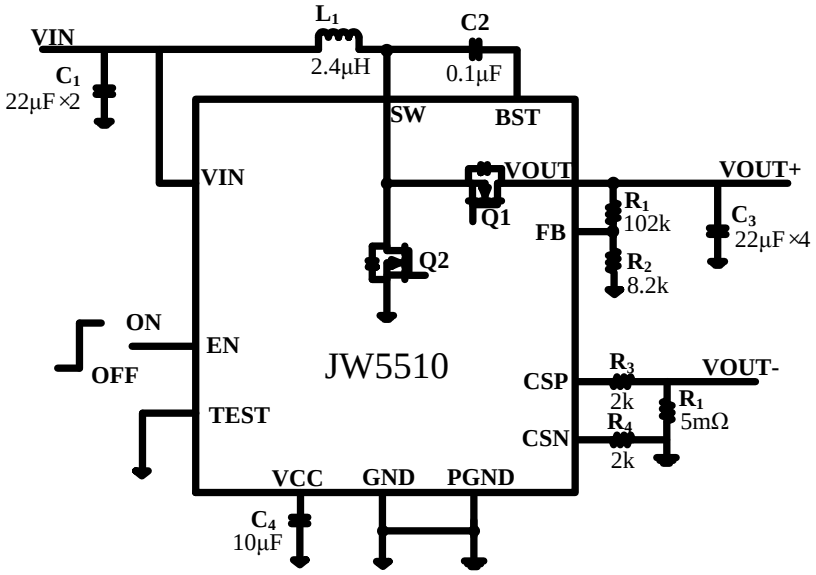
For single cell application we recommend L1=1.2uH.

Reference 2：Output current limit set

V_{IN}: 6.0V ~ 8.4 V

V_{OUT}: 12V

I_{O_LIM}: 4A

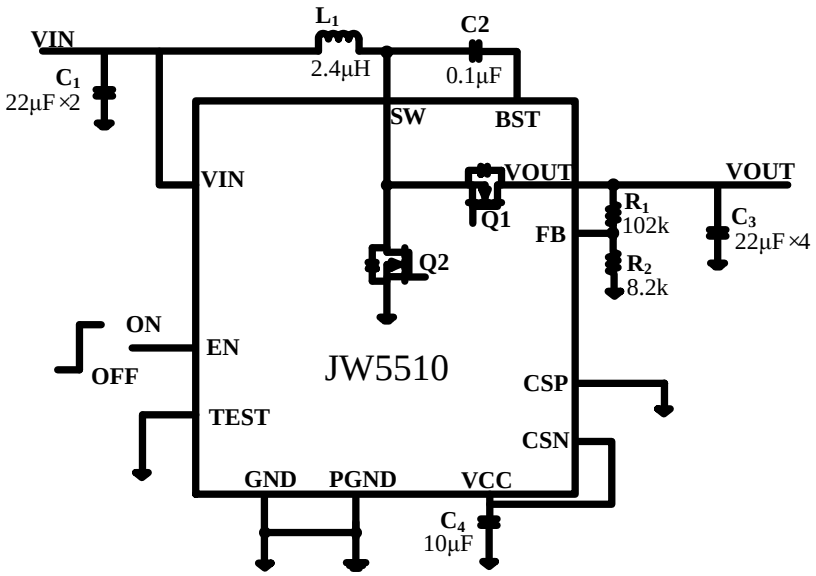


For single cell application we recommend L1=1.2uH.

Reference 3：No current limit set

V_{IN}: 6.0V ~ 8.4 V

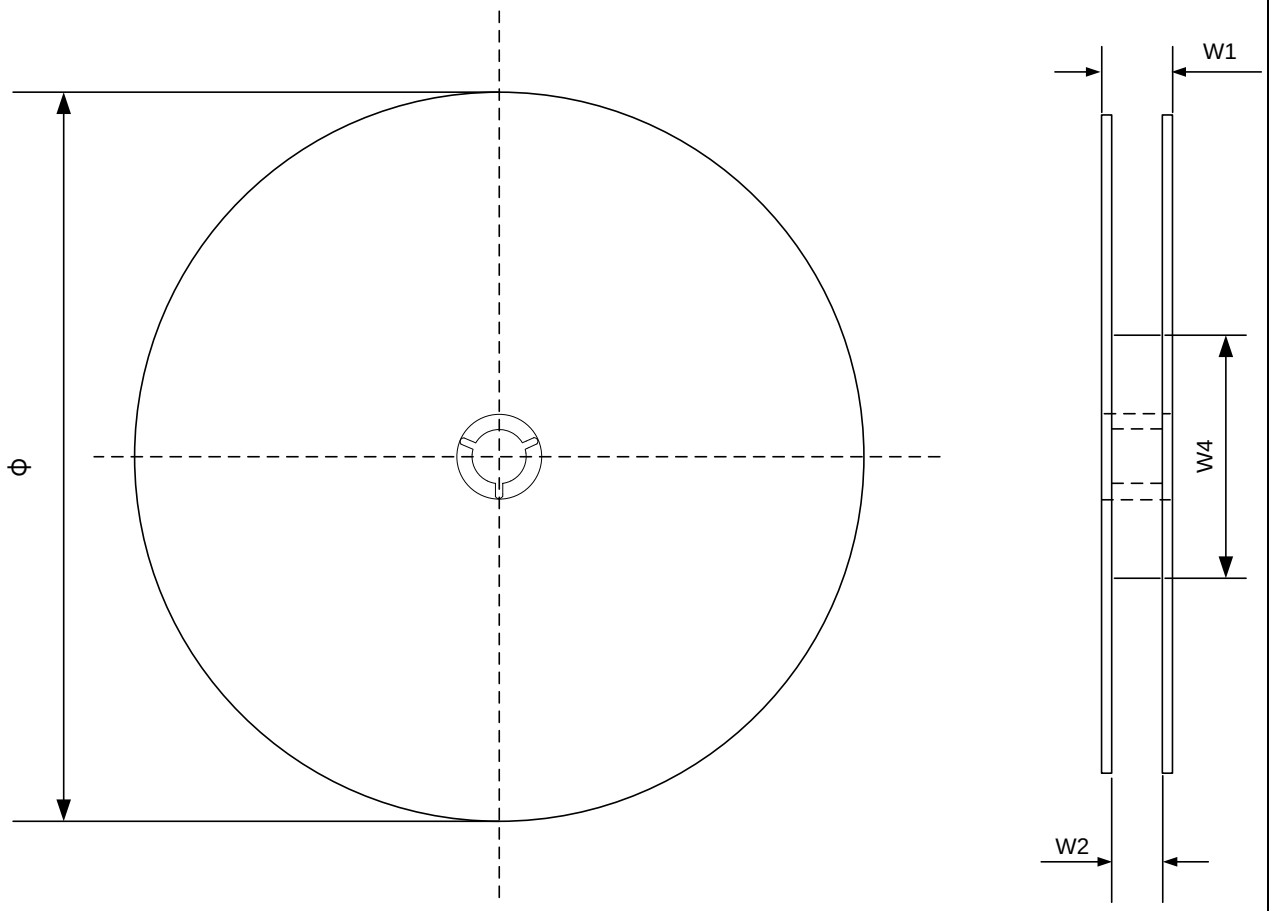
V_{OUT}: 12V



For single cell application we recommend L1=1.2uH.

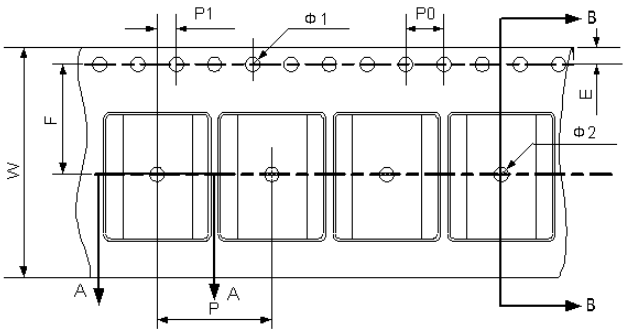
TAPE AND REEL INFORMATION

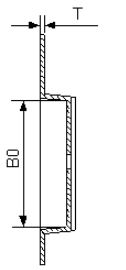
Reel UNIT: mm



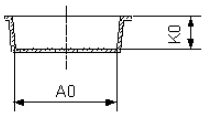
Package	Diameter Φ	Thickness W1	Width W2	W4
DFN3×4-15	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm





SECTION B-B

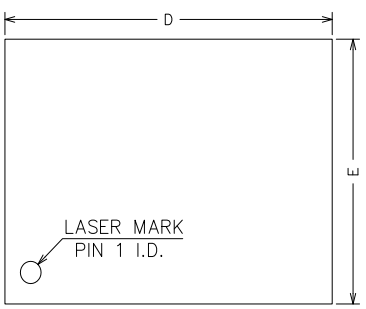


SECTION A-A

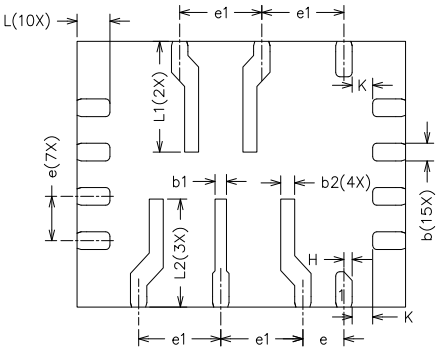
Package	P0	P1	P	A0	B0	W	T0	K0	Φ1	Φ2	E	F
QFN3 x 4-15	4.0±0.1	2.0±0.1	8.0±0.2	3.30±0.2	4.30±0.2	12.0±0.3	0.30±0.20	1.00±0.2	1.55±0.10	1.50min	1.75±0.1	5.50±0.10

PACKAGE OUTLINE

QFN3X4-15 UNIT: mm

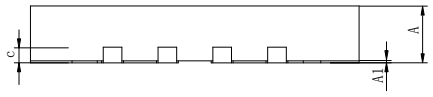


TOP VIEW

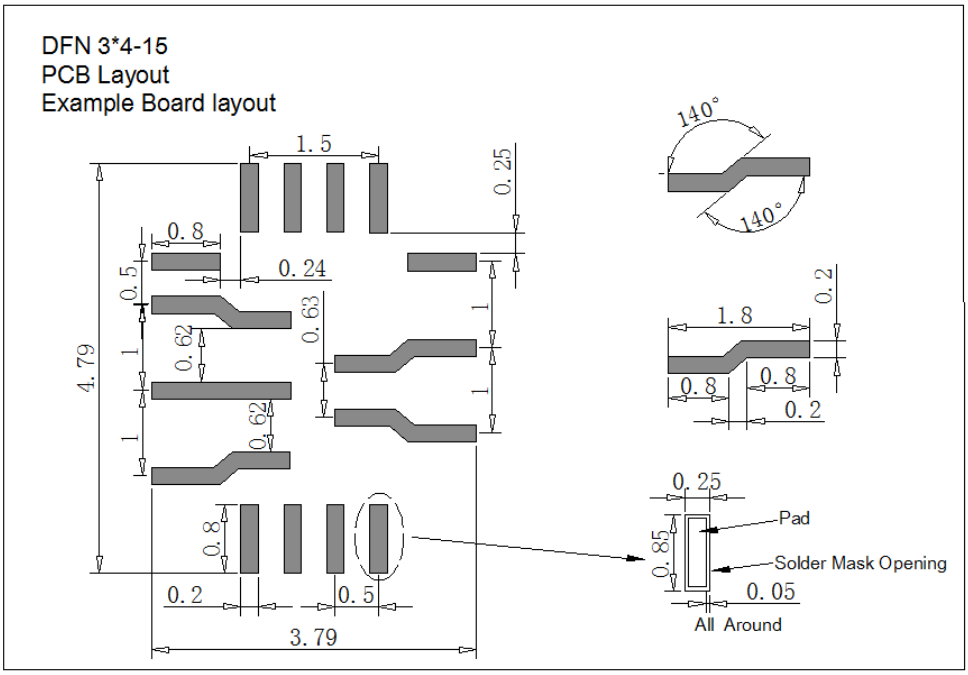


BOTTOM VIEW

	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
c		0.15REF	
b	0.15	0.20	0.25
b1	0.09	0.14	0.19
b2	0.12	0.17	0.22
D	3.90	4.00	4.10
E	2.90	3.00	3.10
e	0.40	0.50	0.60
e1	0.90	1.00	1.10
H		0.10REF	
K	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	1.15	1.25	1.35
L2	1.12	1.22	1.32



SIDE VIEW



Note:

1) All dimensions are in millimeters.
2) Drawing is not to scale.
3) It is recommended to be solder-mask for all pads.
4) Recommended drawing size does not take into account PCB production size error.
5) This drawing is subject to change without notice.

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