JW1602

Multi-topology LED Controller With optimized THD

Parameters Subject to Change Without Notice

DESCRIPTION

The JW®1602 is a multi-topology LED controller with active power factor correction. It is especially designed for LED lighting system. The JW1602 controls the LED current accurately without using an opto-coupler, which can significantly simplify the design of LED lighting system.

The JW1602 achieves high power factor over wide line and load ranges, compared to conventional constant on time control, it also significantly optimized the THD by an improved on time control.

JW1602 integrates an interface for PWM dimming and analog dimming both. The output current can be easily linearly adjusted by an analog signal on ADIM or a PWM signal on DPWM.

The multi-protection function largely enhances the safety and reliability of the system, including over voltage protection, short circuit protection, LED open protection, cycle-by-cycle current limit, VCC UVLO and over-temperature protection.

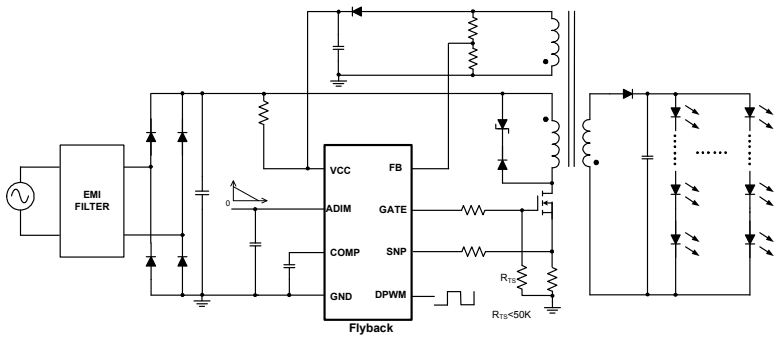
FEATURES

- Real current control without secondary feedback circuit
- Multi-topology supported
- High current accuracy of line regulation
- Active power factor correction
- Optimized THD
- Compatible with analog dimming
- Compatible with PWM dimming
- Frequency fold-back for deep dimming Range
- CV mode to off the LED
- Valley turn-on to low switching loss
- Cycle-by-cycle current limit
- LED short protection
- LED open protection
- Over-temperature protection
- 8-Pin SOP package

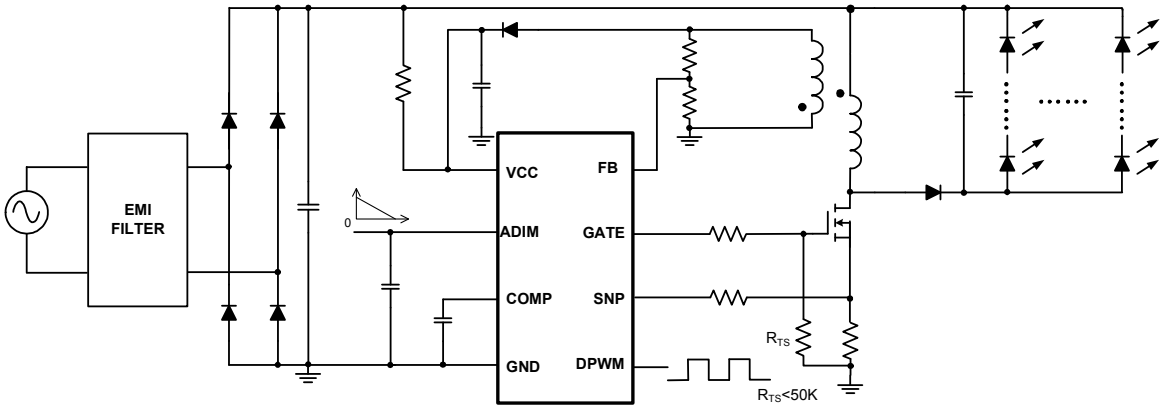
APPLICATIONS

- Offline LED Driver
- Intelligent dimming of LED driver

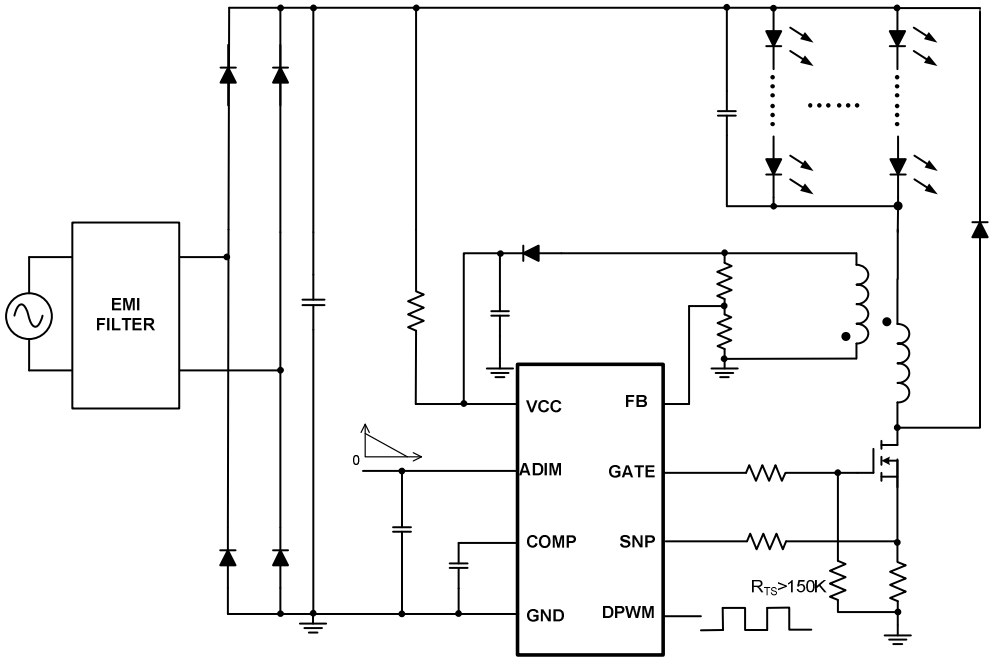
TYPICAL APPLICATION



TYPICAL APPLICATION



Buck-Boost



Buck

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW1602SOPB#TRPBF	SOP8	JW1602 XXXXXXX

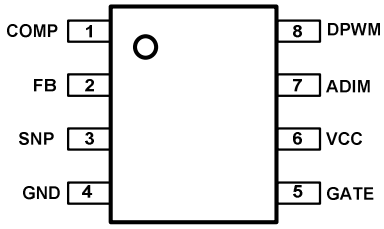
Notes:

1) JW□□□□#TRPBF
   - PB Free
   - Tape and Reel(If "TR" is not shown, it means tube)
   - Package Code
   - Part No.

2) Line 1 of top marking means Part No., and the line 2 of top marking means Date Code.

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VCC PIN 40V
GATE PIN 24V
All Other Pins ..... -0.3V to 5.5V
Junction Temperature[2) 3)] 150ºC
Lead Temperature.....260ºC
Storage Temperature..... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS

VCC PIN .....10V to 30V
FB PIN .....1V to 3V
Junction Temperature (T_J)..... -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{JC}
SOP8	96	45ºC/W

Note:

1) Exceeding these ratings may damage the device.

2) The JW1602 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) The JW1602 includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 25V, T_A = 25ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Vcc Supply(Vcc)						
V_{CC} Turn-On Voltage	V_{CC_ON}		22	24	27	V
V_{CC} Turn-off Low Voltage	$V_{CC\_OFF\_L}$		7.0	8.0	9.5	V
VCC Hysteresis(note1)	V_{CC_HYS}	VCC_ON-VCC_OFF_L		16		V
VCC Shunt Regulator Voltage	$V_{CC\_OFF\_H}$		31	34	37	V
VCC Shunt-off Voltage	$V_{CC\_ON\_H}$		25.5	30	34.5	V
VCC Shunt Regulator Pull-Down Current	I_{CC_PD}	VCC =38V		6		mA
VCC Quiescent Current	I_Q	VCC =20V	15	18	21	μA
V_{CC} Quiescent Current with Switching	I_{Q_SW}	Switching frequency =20kHz; Min on time; Gate floating		500		uA
Sense Current of Primary(SNP)						
V_{REF} Voltage	V_{REF}		294	300	306	mV
SNP Offset voltage(note1)	V_{SNP_OFT}			50		mV
SNP Sense Current Limit(Flyback)	V_{SNP_H1}		1.2	1.5	1.8	V
SNP Sense Current Limit(Buck)	V_{SNP_H2}		1.8	2.2	2.6	V
SNP Inductor Short Current Limit	V_{IND_SHT}		2.2	2.7	3.2	V
Leading Edge Blanking Time(note1)	T_{LEB}			400		ns
Line compensation factor(note1)	K_{LC}			0.04		A/A
Output Feedback(FB)						
FB OVP Threshold	V_{FB_OVP}		3.65	3.8	3.95	V
FB Burst on Threshold in CV	V_{FB_CVON}			1.1		V
FB Burst off Threshold in CV	V_{FB_CVOFF}			1.2		V
FB OVP Sensing blanking time	T_{OVP_BLK1}	SNP>0.6V	1.6	2	2.4	us
FB OVP Sensing blanking time	T_{OVP_BLK2}	SNP<0.3V	0.8	1	1.2	us
Compensation(COMP)						
Comp Max Sourcing Current	I_{SOURCE}			10		uA
Max Comp Voltage(note1)	V_{COMP_H}			4		V
Comp voltage frequency starts to foldback	V_{COMP_FF}			0.8		V
Maximum Oscillator Frequency high	f_{MAX_H}	COMP=1.5V	96	120	145	kHz
Maximum Oscillator Frequency low	f_{MAX_L}	COMP=0.3V	24	30	36	kHz
DPWM Dimming(DPWM)						
DPWM Signal High Level	V_{PWMH}		1.6			V

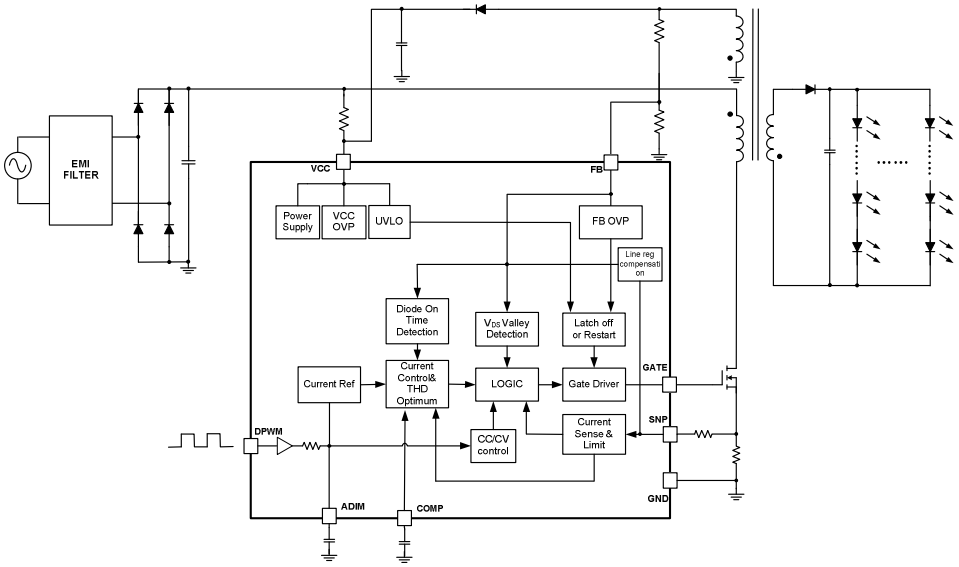
DPWM Signal Low Level	V_{PWML}				0.6	V
Analog Dimming(ADIM)						
ADIM OFF	V_{ADIM_OFF}			0.2		V
ADIM Low threshold voltage	V_{ADIM_LOW}			0.3		V
ADIM HIGH threshold voltage	V_{ADIM_HIGH}			3.3		V
Gate output(GATE)						
Gate Output High	V_{GATE_H}		9.6	12	14.4	V
Gate Output Low	V_{GATE_L}				200	mV
t_r Gate Driver Output Rise Time	T_{GATE_R}	C_L=1nF 1V to 8V		50		ns
t_f Gate Driver Output Fall Time	T_{GATE_F}	C_L=1nF 8V to 1V		50		ns
Maximum turn on time	T_{on_max}		30	40		us
Minimum turn on time	T_{on_min}		360	450	540	ns
Maximum turn off time	T_{off_max}		160	200	240	us
Thermal						
Thermal foldback Temperature(note1)	T_{OTPFB}			140		℃

Note1: Guarantee by design.

PIN DESCRIPTION

Pin	Name	Description
1	COMP	Compensation Pin for Internal Error Amplifier. Connect a capacitor between the pin and GND to compensate the internal feedback loop.
2	FB	Voltage Loop Feedback Pin. VFB is used to detect open LED conditions by sampling the auxiliary winding voltage.
3	SNP	Primary current sense Pin. The pin is used for cycle-by-cycle peak current control and limit.
4	GND	Power Ground.
5	GATE	Gate Driver for the External Main MOSFET Switch.
6	VCC	Power Supply Pin. This pin supplies current to the internal start-up circuit. This pin must be bypassed with a capacitor nearby.
7	ADIM	Apply an analog signal on this pin for analog dimming, CV mode take the control loop if ADIM goes below than 0.2V. An external capacitor should be connected on ADIM to filter out the DPWM to get the internal current reference.
8	DPWM	Apply a PWM signal on this pin for external PWM dimming.

BLOCK DIAGRAM

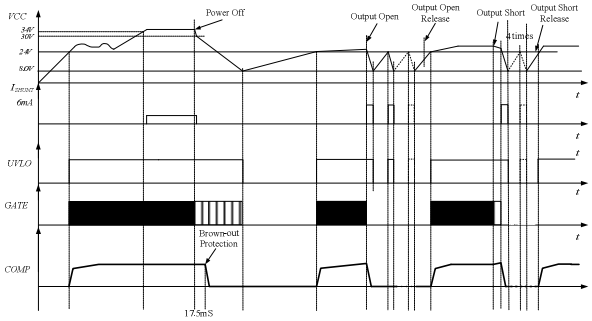


FUNCTIONAL DESCRIPTION

The JW1602 is a multi-topology LED controller optimized for LED lighting. It uses a novel method to calculate the output current without the need of opto-coupler. The JW1602 achieves high power factor over wide line and load ranges, compared to conventional constant on time control, it also significantly optimized the THD by a improved on time control.

Start Up

The JW1602 uses a hysteretic start-up to operate from high offline voltages. A resistor connected to the supply voltage protects the part from high voltages. When the DC line charges VCC up to 24V, the gate drive signal begins to switch. The auxiliary winding provides power to the VCC pin along with the resistor in steady state. The gate turns off if VCC goes below than 8V. An internal voltage clamp helps to prevent VCC from being too high. When VCC goes above 34V, an internal shunt current regulates the Vcc voltage. The shunt stops pulling down when VCC is lower than 30V.



Vcc Timing Diagram

Primary-Side Current Control

The JW1602 controls the output current from the information of inductor current. The output LED means current can be calculated as:

$$I_O = \begin{cases} \dfrac{V_{REF} \cdot N_{PS}}{2R_S} & \text{For Flyback} \\ \dfrac{V_{REF}}{2R_S} & \text{For Buck-Boost} \\ \dfrac{V_{REF}}{R_S} & \text{For Buck} \end{cases}$$

Where

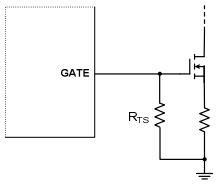
N_{PS} – Turns ratio of primary winding to secondary winding;

V_{REF}– Reference voltage, 300mV typically;

R_S – Sensing resistor connected between SNP and ground.

Multi-Topology Operation Principle

JW1602 supports multi-topology operation with only one resistor R_{TS} that connected between GATE pin and GND pin.



JW1602 works in BUCK mode when R_{TS} is larger than 150Kohm (floating included), and in Buck-Boost/Flyback mode when R_{TS} is smaller than 50Kohm.

Improved COT control to optimize THD

The JW1602 integrates an improved COT control circuit to optimize THD in BUCK-Boost/Flyback mode.

The average input current can be deduced as,

$$I_{in} = \frac{\sqrt{2} \cdot Vac \cdot \sin(t)}{2L} \cdot T_{on} \cdot D(t)$$

Where Ton is the on-time of GATE, D(t) is the duty cycle.

The dedicated THD improved circuit can modulate input current as a pure sinusoidal wave,

$$I_{in} = k \sin(t)$$

Here k is a constant.

Line Regulation Compensation Design

The gate turn-off delay is the main reason that causes bad line regulation, the increased voltage on SNP by delay Td can be expressed as,

$$\Delta V_{SNP} = \frac{V_{IN}}{L_m} T_d R_S$$

Here, RS is the sensing resistor. Td is the total turn-off delay of power MOSFET.

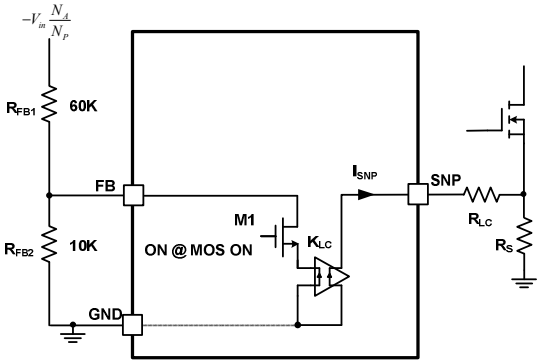
To compensate this increased current of primary side, a current I_{SNP} which is proportional to the voltage on auxiliary winding, sourced from the SNP pin and flows through resistor R_{LC}, the sourcing current is,

$$I_{SNP} = K_{LC} \frac{N_A \cdot V_{in}}{N_P \cdot R_{FB1}}$$

Where, N_A is the turns of auxiliary winding, N_P is the turns of primary winding and K_{LC} is current factor, 0.04A/A.

The RLC can be designed as,

$$R_{LC} = \frac{\Delta V_{SNP}}{I_{SNP}} = \frac{T_d \cdot R_S \cdot N_P \cdot R_{FB1}}{K_{LC} \cdot N_A \cdot L_m}$$



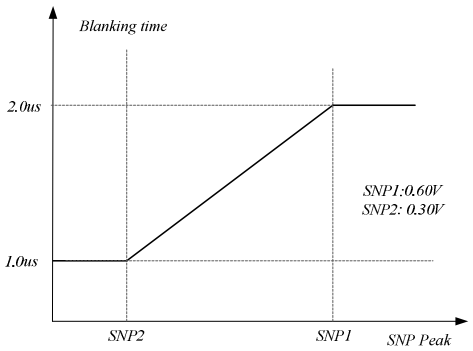
Line regulation compensation circuit

Critical Conduction Mode Operation

Critical conduction mode is a variable frequency switching scheme that always returns the secondary current to zero in each cycle. The JW1602 relies on this mode to calculate the output current. When the external MOSFET turns off, the energy stored in the inductor forces the secondary freewheeling diode to turn on, and the current of the inductor begins to decrease linearly from peak to zero. When the current decreases to zero, the resonance, caused by the inductor and all the parasitic capacitance, makes the MOSFET drain-source voltage decreases, this decreasing can also be reflected at the auxiliary winding. The turn on signal is generated when the drain-source voltage is approximately at the valley. This switching technique can reduce the MOSFET turn-on losses and diode reverse recovery losses, thus improves efficiency and decreases EMI noise.

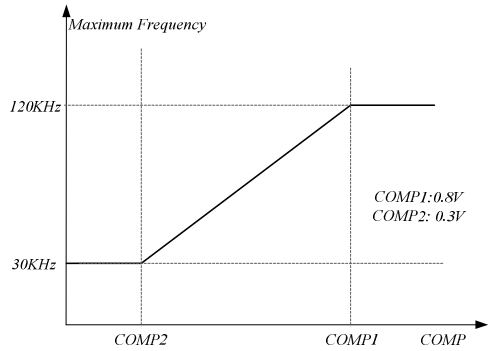
Adaptive Blanking Time for FB Voltage Sensing

To filter out the noise on FB and to get an accurate FB voltage via the auxiliary winding, a blanking time is inserted after the MOSFET turns off. The blanking time is modulated by the SNP peak. The minimum blanking time is about 1us, the maximum is about 2.0us.



Maximum Frequency Fold-back

JW1602 integrates a maximum frequency fold-back mechanism based on COMP voltage, which ensures a deep dimming. It starts to reduce the maximum frequency when COMP <0.8V and ends at 30KHz when COMP goes down to 0.3V.

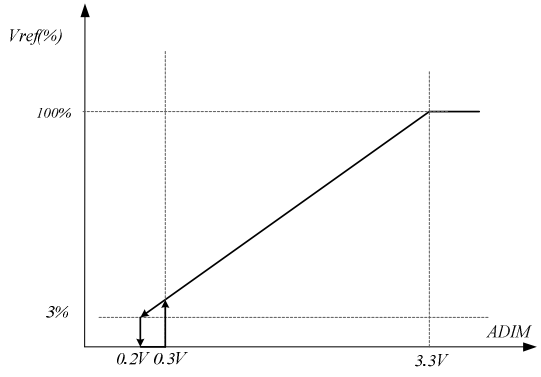


Loop Compensation

An integrator is applied to the output current feedback loop with a capacitor connected to the COMP. For offline applications, the crossover frequency should be set much less than the line frequency of 120Hz or 100Hz. To have a good PFC performance, a capacitor of 1μF connected to COMP is recommended.

Analog Dimming

JW1602 incorporates the analog dimming function. An analog signal can be applied to ADIM pin, it can linearly change the internal current reference according to the ADIM which is between V_{ADIM_LOW} and V_{ADIM_HIGH}. It can achieve about 3%~100% dimming range.

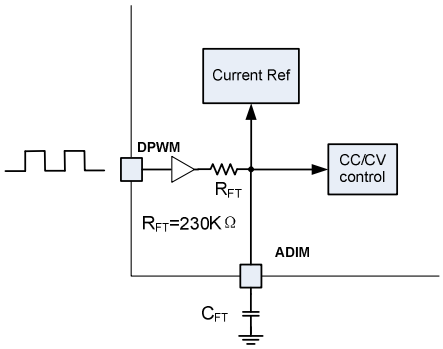


The output current decreases linearly when the ADIM voltage decreases from 3.3V to 0.2V. As soon as ADIM<0.2V, CV loop takes the control loop thus makes the LED in totally off state. When ADIM voltage increases from <0.2V, CC mode will not take the control loop until ADIM≥0.3V.

For non-dimming applications, a bypass ceramic cap should be applied to ADIM pin, <10nF in usual.

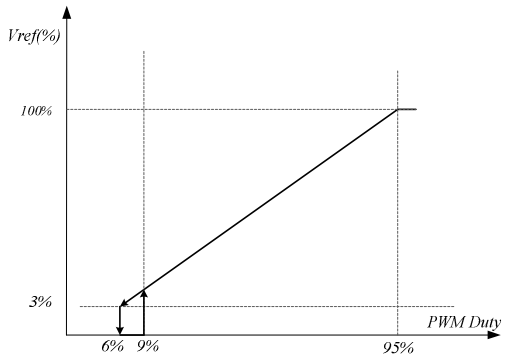
PWM Dimming

When the PWM signal is injected to DPWM, The PWM signal is conditioned and filtered by a bypass capacitor on ADIM. The internal current reference is adjusted by ADIM, so that the output current is proportional to the PWM duty cycle.



To have a higher PF, lower THD the time constant of $R_{FT}C_{FT}$ should be larger enough to filter the PWM signal to a DC value.

$$R_{FT}C_{FT} \approx 3\sim5\ T_{PWM}$$

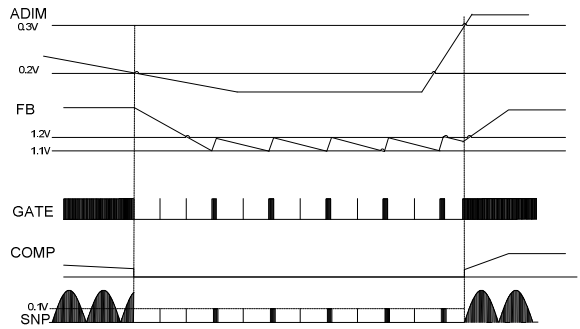


The output current decreases linearly when the PWM duty cycle decreases from 100% to 6%. As soon as duty <6%, CV loop takes the control loop thus makes the LED in totally off state. When the PWM duty increases from <6%, CC

mode will not take the control loop until the duty ≥9%.

CV mode

CV mode takes the control loop if ADIM goes below than 0.2V, and returns to CC control when ADIM is over than 0.3V.
When FB voltage goes below 1.1V, it starts to switch with peak current control, and the SNP peak voltage is controlled at 0.1V. It stops switching for 1.7mS when detected FB ramp up over 1.2V.



LED Over Temperature Protection

When JW1602 is hotter than 140°C, the internal current reduces linearly in order to reduce the output current. When the temperature is higher than 160°C, the output current reduces to <30% of the rated.

Brown-out Protection

When the peak SNP voltage is lower than 50mV and lasts for 17.5ms, Brown-out protection could be triggered, then COMP is pulled down zero.

LED Open Protection

The output voltage can reflect on the auxiliary winding when the main power switch is off. A resistor divider from the auxiliary winding is connected to the FB pin. FB voltage could be detected with an OVP blanking time after the main MOSFET turns off. If the FB voltage is higher than 3.8V, LED open protection could be triggered and the GATE stops switching, and Vcc is pulled down to 8V by an internal sink current and then charged to 24V by the external resistor, which repeats for four times of discharging and charging of Vcc before the next detection cycle.

LED Short Protection

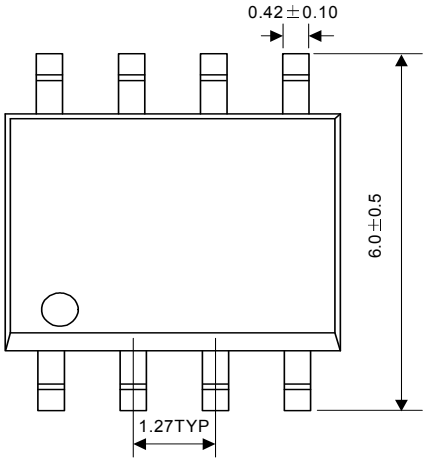
When the output is shorted, the auxiliary winding voltage comes to zero. JW1602 counts this state for 100ms, if short goes on, it stops switching and set a FAULT flag. Vcc is pulled down to 8V by an internal sink current and then is charged to 24V by the external resistor, which repeats for four times of discharging and charging of Vcc before the next detection cycle.

PCB Guidelines

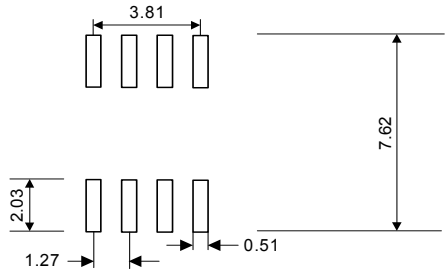
1. The bypass ceramic capacitor of VCC should be nearby the VCC and GND as close as possible.
2. To reduce EMI noise, the power loop area should be as small as possible.
3. JW1602 should be kept away from noisy and heating components, such as MOSFET, transformer and diode.
4. FB pin should be kept away from sources of interference; a 20pF capacitor could be paralleled if necessary.

PACKAGE OUTLINE

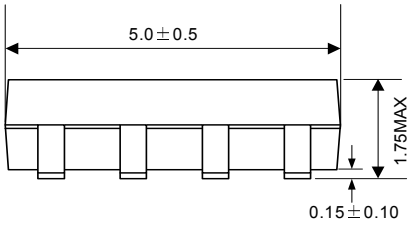
SOP8 UNIT: mm



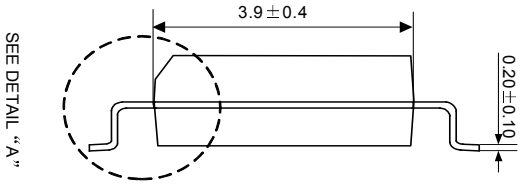
TOP VIEW



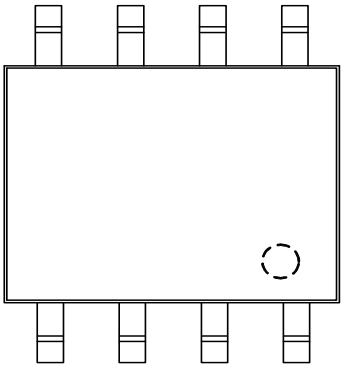
RECOMMENDED LAND PATTERN



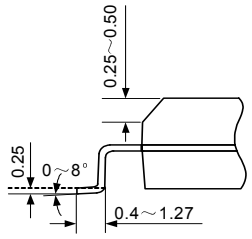
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

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