

High Voltage half bridge driver

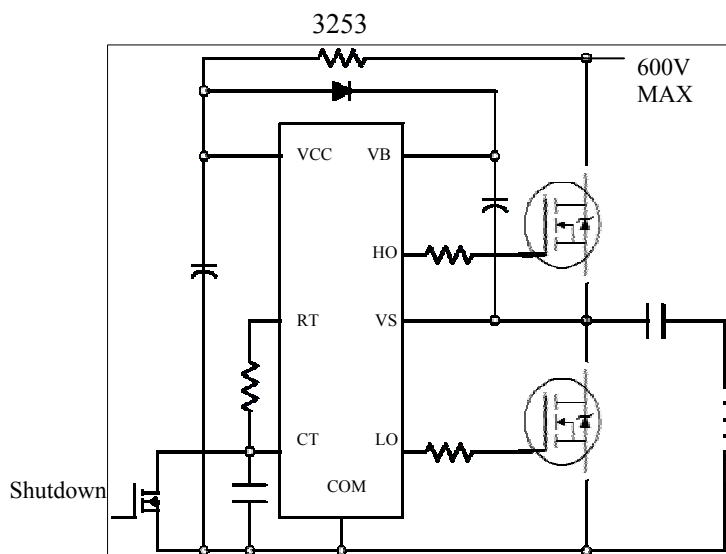
General Description

The 3253 are an high voltage half bridge driver which incor-porates a high voltage half-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. The 3253 provides more functionality and is easier to use. A shutdown feature has been designed into the CT pin, so that both gate driver outputs can be disabled using a low voltage control signal. In addition, the gate driver output pulse widths are the same once the rising undervoltage lockout threshold on VCC has been reached, resulting in a more stable profile of frequency vs time at startup. Noise immunity has been improved significantly, both by lowering the peak di/dt of the gate drivers, and by increasing the undervoltage lockout hysteresis to 1V. Finally, special attention has been paid to maximizing the latch immunity of the device, and providing comprehensive ESD protection on all pins.

Key Features

- Integrated 600V half-bridge gate driver
- 15.6V zener clamp on Vcc
- True micropower start up
- Tighter initial deadtime control
- Low temperature coefficient deadtime
- Shutdown feature (1/6th Vcc) on CT pin
- Increased undervoltage lockout Hysteresis (1V)
- Lower power level-shifting circuit
- Constant LO, HO pulse widths at startup
- Lower di/dt gate driver for better noise immunity
- Low side output in phase with RT
- Excellent latch immunity on all inputs and outputs
- ESD protection on all leads
- Also available LEAD-FREE

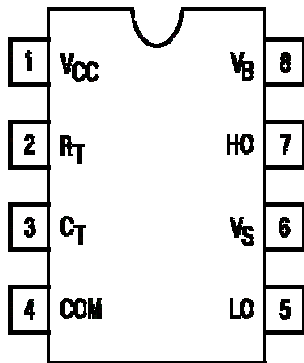
Typical Application



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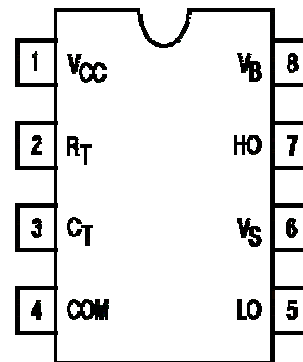
Pin Assignments

3253P



8 Lead PDIP

3253S



8 Lead SOIC

Absolute Maximum Ratings

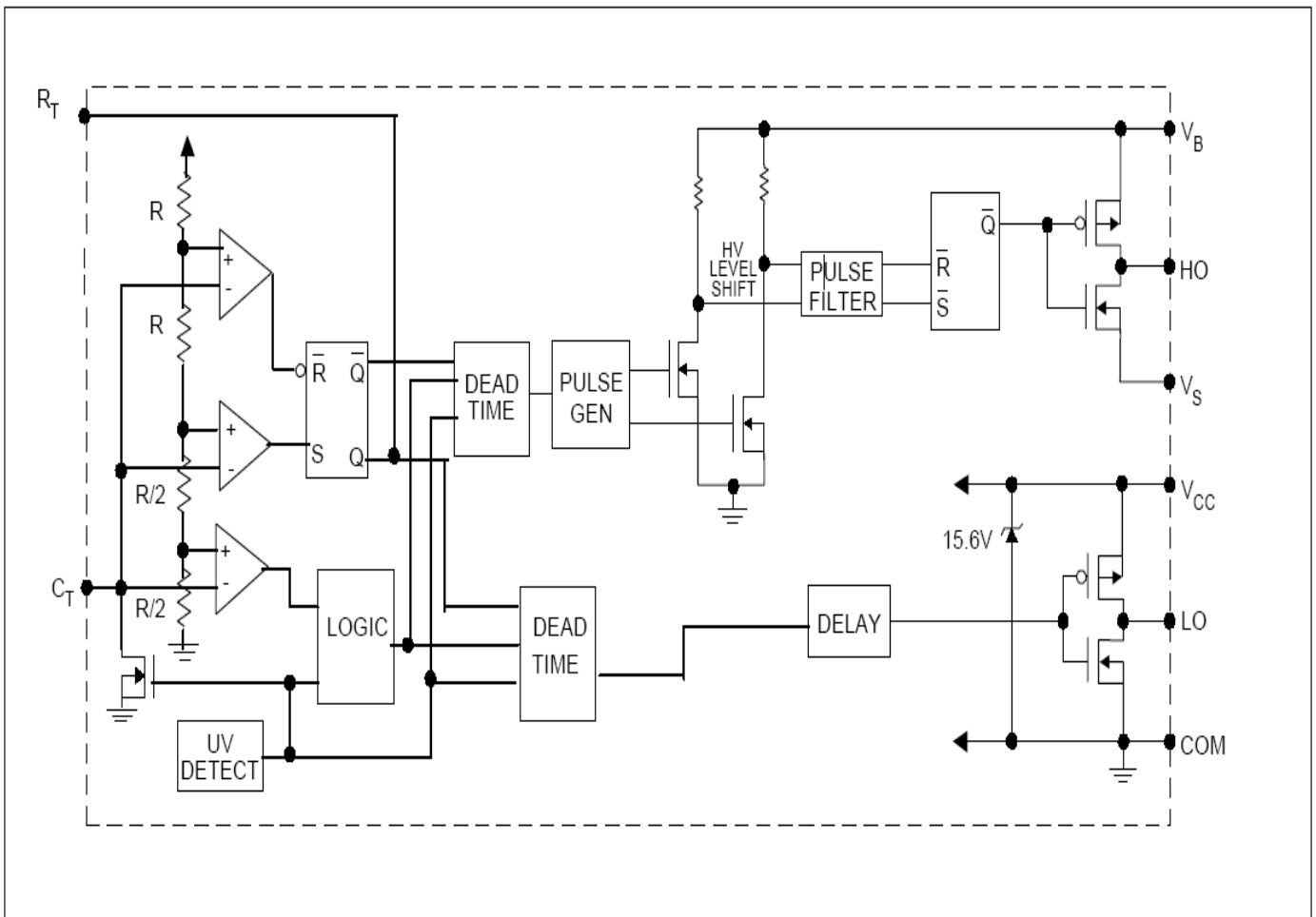
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
VB	High side floating supply voltage	-0.3	625	V	
VS	High side floating supply offset voltage	VB - 25	VB + 0.3		
VHO	High side floating output voltage	VS - 0.3	VB + 0.3		
VLO	Low side output voltage	-0.3	VCC + 0.3		
VRT	RT pin voltage	-0.3	VCC + 0.3		
VCT	CT pin voltage	-0.3	VCC + 0.3		
ICC	Supply current (note 1)	—	25	mA	
IRT	RT pin current	-5	5		
dVs/dt	Allowable offset voltage slew rate	-50	50	V/ns	
PD	Maximum power dissipation @ TA ≤ +25°C	(8 Lead DIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
RthJA	Thermal resistance, junction to ambient	(8 Lead DIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
TJ	Junction temperature	-55	150	°C	
TS	Storage temperature	-55	150		
TL	Lead temperature (soldering, 10 seconds)	—	300		

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Block Diagram

Functional Block Diagram for 3253



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Electrical Characteristic

$V_{BIAS}(V_{CC}, V_{BS}) = 12V$, $CL = 1000\text{ pF}$, $CT = 1\text{ nF}$ and $TA = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_o and I_o parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Low Voltage Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	Rising V_{CC} undervoltage lockout threshold	8.1	9.0	9.9	V	
V_{CCUV-}	Falling V_{CC} undervoltage lockout threshold	7.2	8.0	8.8		
V_{CCUVH}	V_{CC} undervoltage lockout Hysteresis	0.5	1.0	1.5		
I_{QCCUV}	Micropower startup V_{CC} supply current	—	75	150	μA	$V_{CC} \leq V_{CCUV-}$
I_{QCC}	Quiescent V_{CC} supply current	—	500	950		
V_{CLAMP}	V_{CC} zener clamp voltage	14.4	15.6	16.8	V	$I_{CC} = 5\text{mA}$
Floating Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{QBSUV}	Micropower startup V_{BS} supply current	—	0	10	μA	$V_{CC} \leq V_{CCUV-}$
I_{QBS}	Quiescent V_{BS} supply current	—	30	50		
V_{BSMIN}	Minimum required V_{BS} voltage for proper functionality from RT to HO	—	4.0	5.0	V	$V_{CC} = V_{CCUV+} + 0.1\text{V}$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600\text{V}$
Oscillator I/O Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
fosc	Oscillator frequency	19.4	20	20.6	kHz	$RT = 36.9\text{k}\Omega$
		94	100	106		$RT = 7.43\text{k}\Omega$
d	RT pin duty cycle	48	50	52	%	$f_o < 100\text{kHz}$
ICT	CT pin current	—	0.001	1.0	μA	
ICTUV	UV-mode CT pin pulldown current	0.30	0.70	1.2	mA	$V_{CC} = 7\text{V}$
VCT+	Upper CT ramp voltage threshold	—	8.0	—	V	
VCT-	Lower CT ramp voltage threshold	—	4.0	—		
VCTSD	CT voltage shutdown threshold	1.8	2.1	2.4		
VRT+	High-level RT output voltage, $V_{CC} - V_{RT}$	—	10	50	mV	$I_{RT} = 100\mu\text{A}$ $I_{RT} = 1\text{mA}$
		—	100	300		
VRT-	Low-level RT output voltage	—	10	50		$I_{RT} = 100\mu\text{A}$ $I_{RT} = 1\text{mA}$
		—	100	300		
VRTUV	UV-mode RT output voltage	—	0	100		$V_{CC} \leq V_{CCUV-}$
VRTSD	SD-Mode RT output voltage, $V_{CC} - V_{RT}$	—	10	50		$I_{RT} = 100\mu\text{A}$ $V_{CT} = 0\text{V}$
		—	10	300	$I_{RT} = 1\text{mA}$ $V_{CT} = 0\text{V}$	

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Electrical Characteristic

(Continued)

Gate Driver Output Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
VOH	High level output voltage, VBIAS -Vo	—	0	100	mV	Io = 0A
VOL	Low-level output voltage, VO	—	0	100		Io = 0A
VOL_-UV	UV-mode output voltage, VO	—	0	100		Io=0A Vcc ≤ Vccuv-
tr	Output rise time	—	80	150	nsec	
tf	Output fall time	—	45	100		
tsd	Shutdown propagation delay	—	660	—		
td	Output deadtime (HO or LO)	0.75	1.20	1.65	μsec	

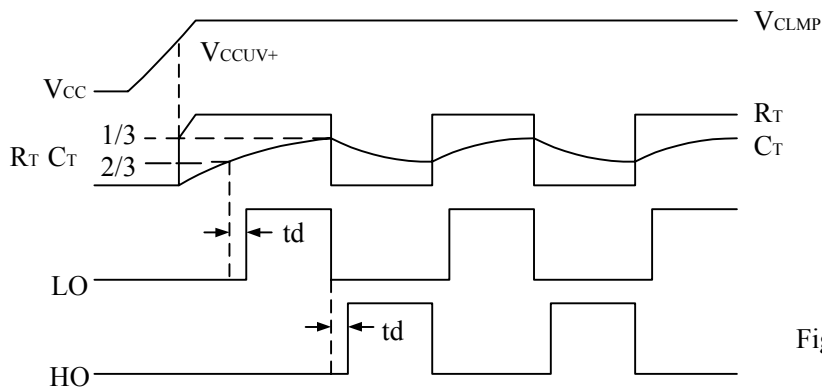


Figure 1. Input/Output Timing Diagram

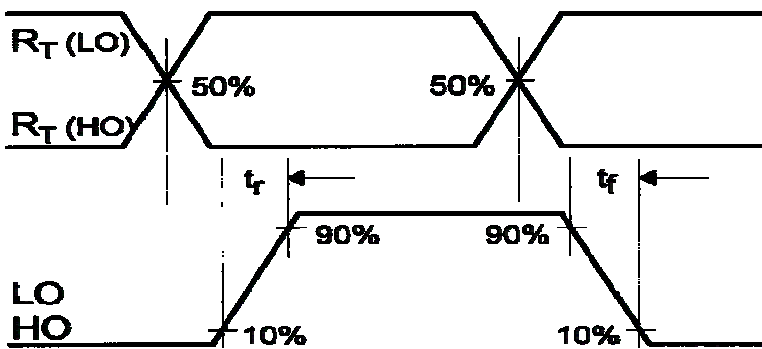


Figure 2. Switching Time Waveform Definitions

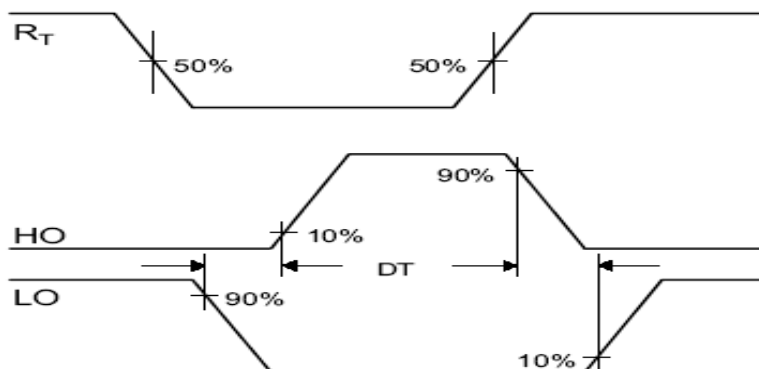


Figure 3. Deadtime Waveform Definitions

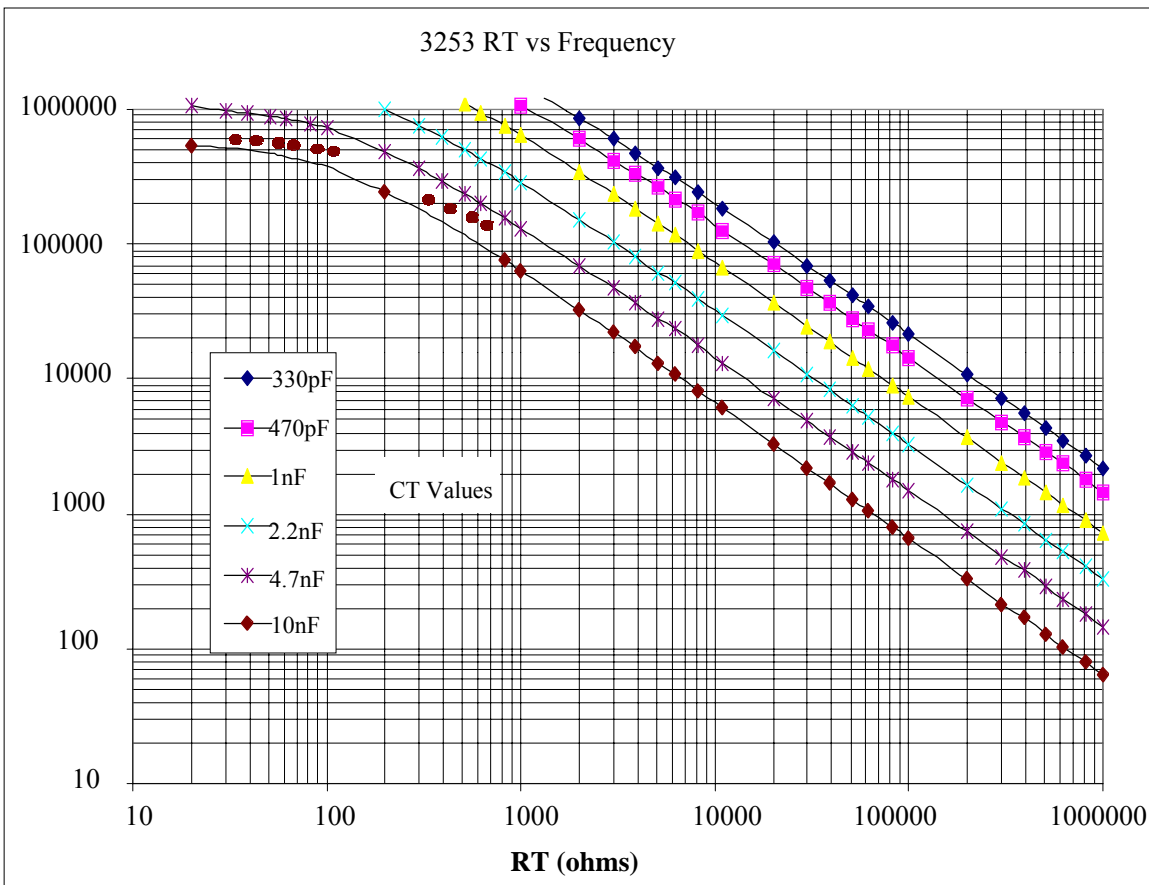
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Ordering Information

Leadfree Part	Leadfree Part
8-Lead PDIP 3253P order 3253P	8-Lead SOIC 3253S order 3253S

Recommended Component Values

Symbol	Component	Min.	Max.	Units
RT	Timing resistor value	10	—	kΩ
CT	CT pin capacitor value	330	—	pF



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Mechanical Dimensions

