

BT169D-L

SCR

Rev. 6 — 20 March 2012

Product data sheet

1. Product profile

1.1 General description

Planar passivated very sensitive gate Silicon Controlled Rectifier in a SOT54 (TO-92) plastic package.

1.2 Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Very sensitive gate

1.3 Applications

- Ignition circuits
- Low power latching circuits
- Protection / shut-down circuits: lighting ballasts
- Protection / shut-down circuits: Switched Mode Power Supplies

1.4 Quick reference data

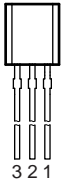

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	400	V
V_{RRM}	repetitive peak reverse voltage		-	-	400	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 10\text{ ms}$; see Figure 4 ; see Figure 5	-	-	8	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{\text{lead}} \leq 83\text{ °C}$; see Figure 1 ; see Figure 2	-	-	0.8	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; see Figure 7	-	-	50	μA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; see Figure 9	-	0.4	1	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.5\text{ mA}$; $T_j = 25\text{ °C}$; see Figure 8	-	2	4	mA



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode		 sym037
2	G	gate		
3	K	cathode		

SOT54 (TO-92)

3. Ordering information

Table 3. Ordering information

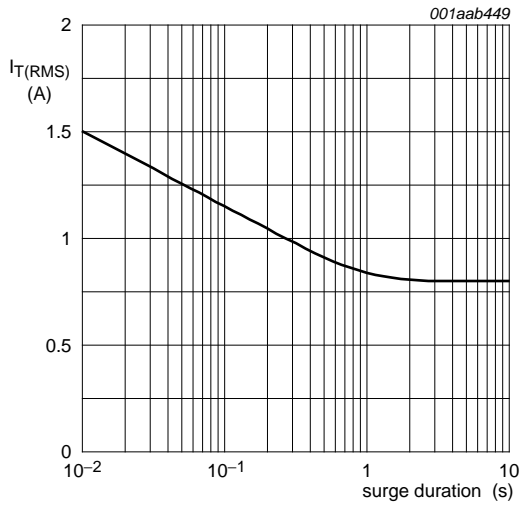
Type number	Package		
	Name	Description	Version
BT169D-L	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

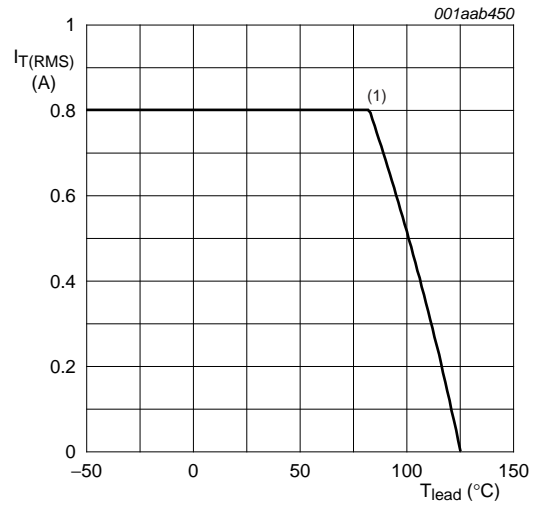
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$; see Figure 3	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$; see Figure 1 ; see Figure 2	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	9	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; see Figure 4 ; see Figure 5	-	8	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	0.32	A ² s
di_T/dt	rate of rise of on-state current	$I_T = 2\text{ A}$; $I_G = 10\text{ mA}$; $di_G/dt = 100\text{ mA}/\mu\text{s}$	-	50	A/ μs
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C



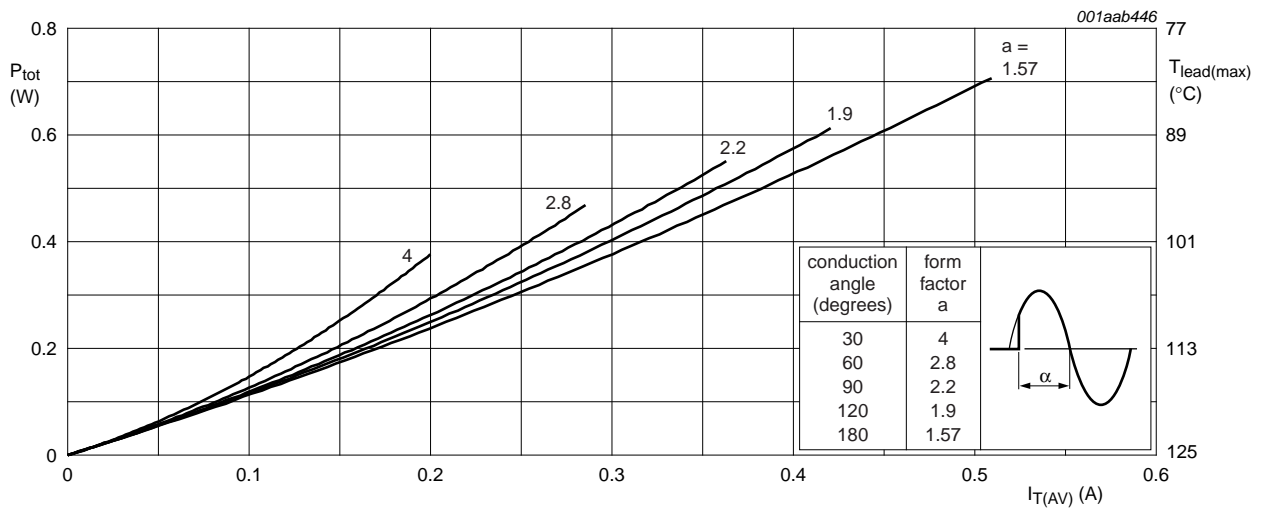
$f = 50\text{Hz}; T_{\text{lead}} \leq 83^\circ\text{C}$

Fig 1. RMS on-state current as a function of surge duration for sinusoidal currents



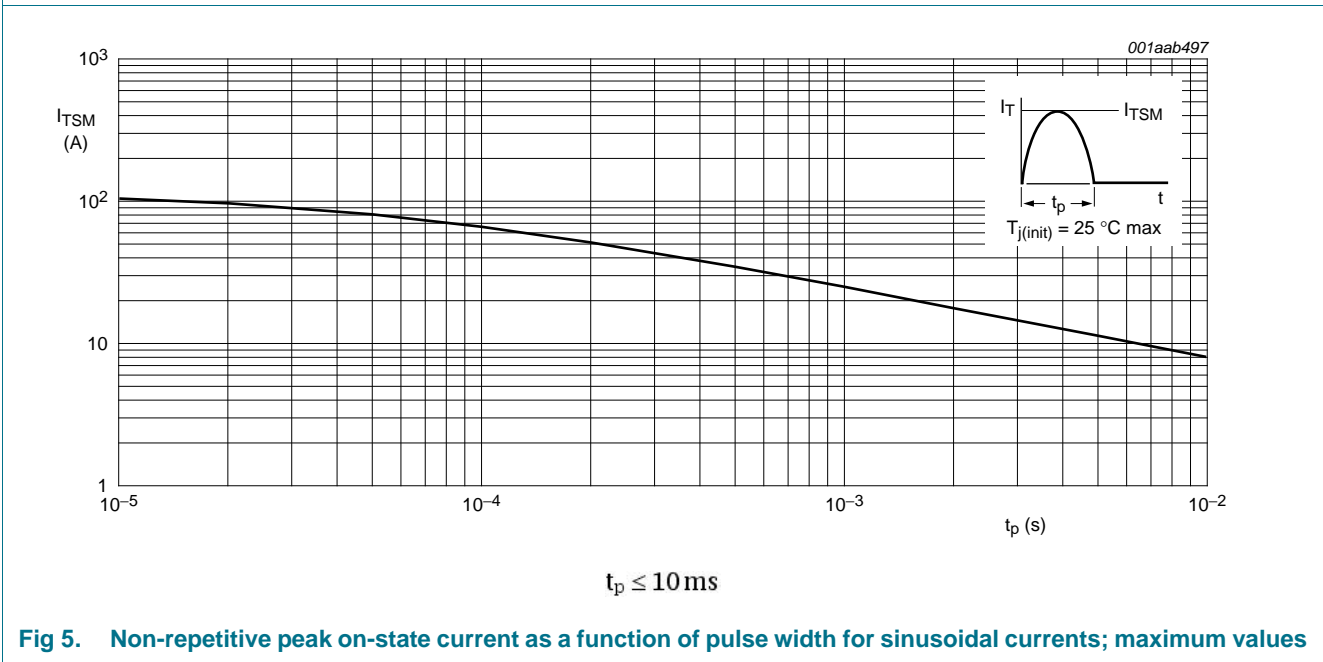
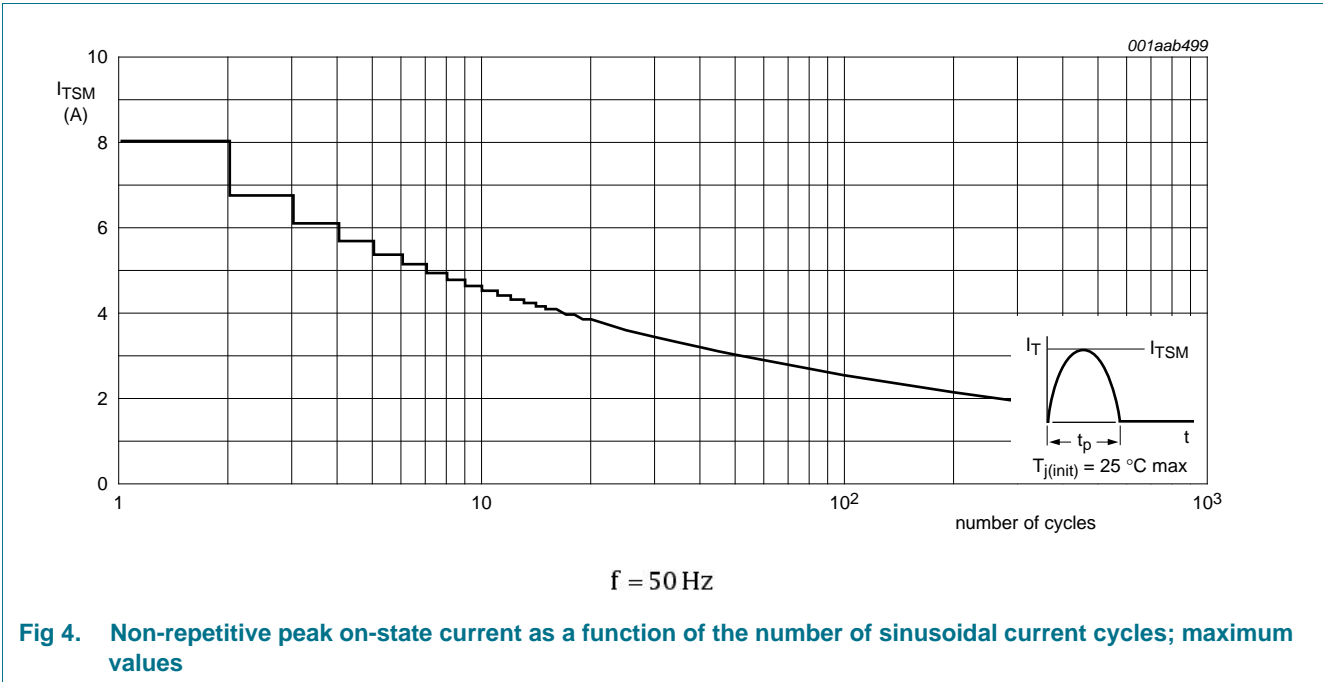
(1) $T_{\text{lead}} = 83^\circ\text{C}$

Fig 2. RMS on-state current as a function of lead temperature; maximum values



$$\text{Form factor } a = \frac{I_T(\text{RMS})}{I_T(\text{AV})}$$

Fig 3. Total power dissipation as a function of average on-state current; maximum values



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W

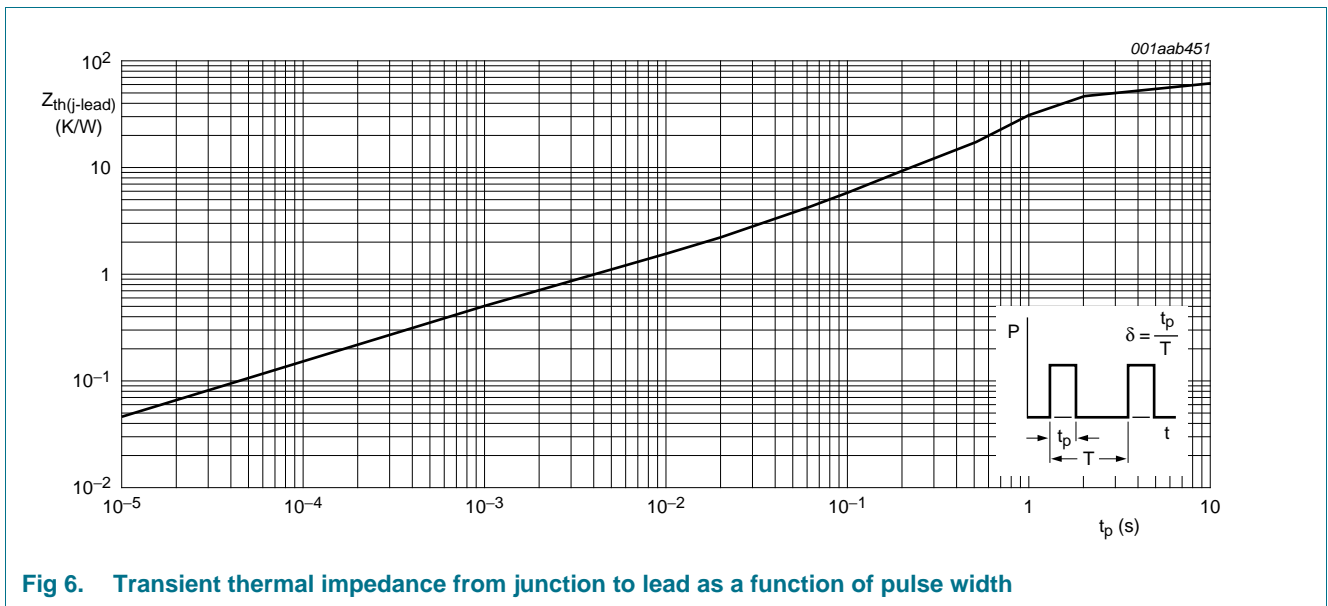
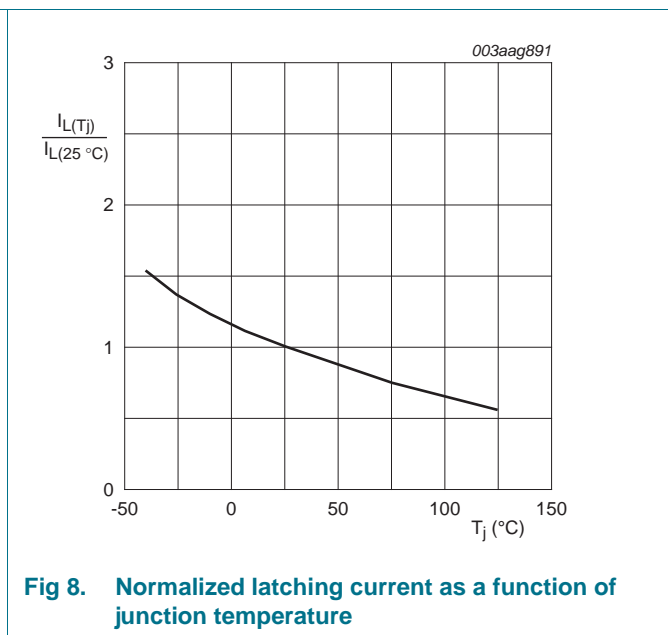
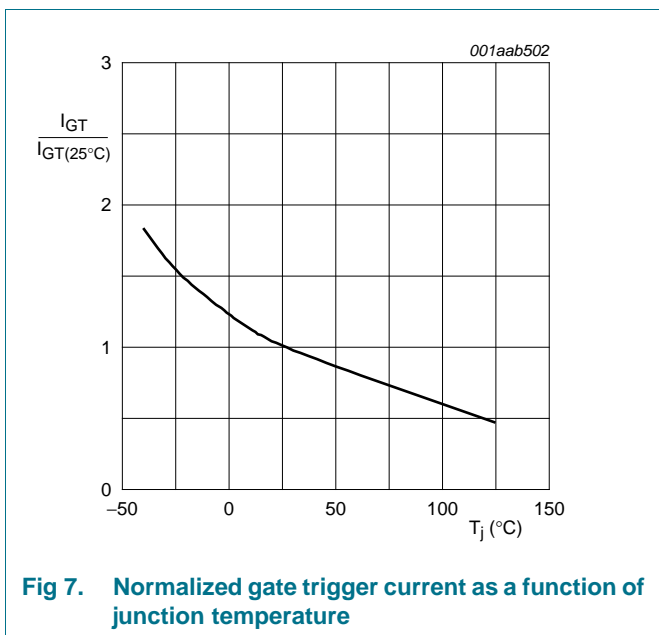


Fig 6. Transient thermal impedance from junction to lead as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	50	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.5\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 8	-	2	4	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 9	-	0.4	1	mA
V_T	on-state voltage	$I_T = 1.2\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 10	-	1.25	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 11	-	0.5	0.8	V
		$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 125\text{ }^\circ\text{C}$; see Figure 11	0.2	0.3	-	V
I_D	off-state current	$V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	mA
		$V_D = 400\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$	-	-	2	μA
I_R	reverse current	$T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; $V_R = 400\text{ V}$	-	0.05	0.1	mA
		$T_j = 25\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; $V_R = 400\text{ V}$	-	-	2	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 268\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; exponential waveform; see Figure 12	500	800	-	$\text{V}/\mu\text{s}$
		$V_{DM} = 268\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; exponential waveform; gate open circuit; see Figure 12	-	25	-	$\text{V}/\mu\text{s}$



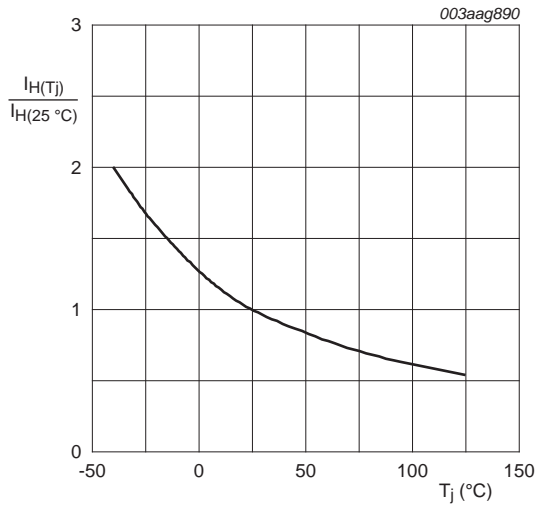
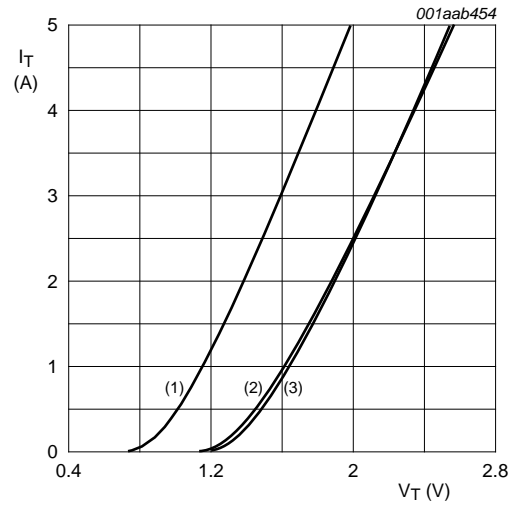


Fig 9. Normalized holding current as a function of junction temperature



$V_o = 1.067 \text{ V}; R_s = 0.187 \Omega$

- (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
- (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
- (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig 10. On-state current as a function of on-state voltage

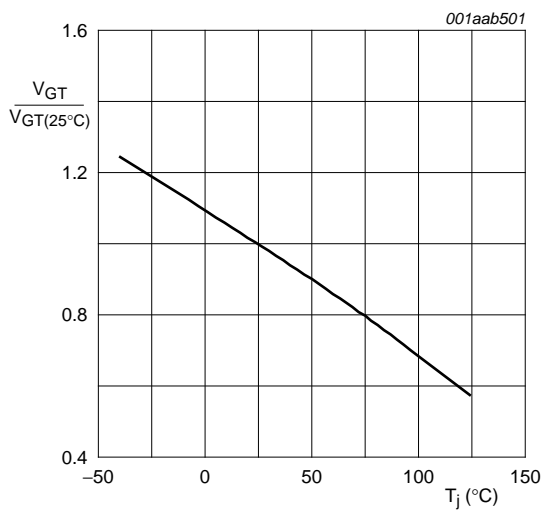
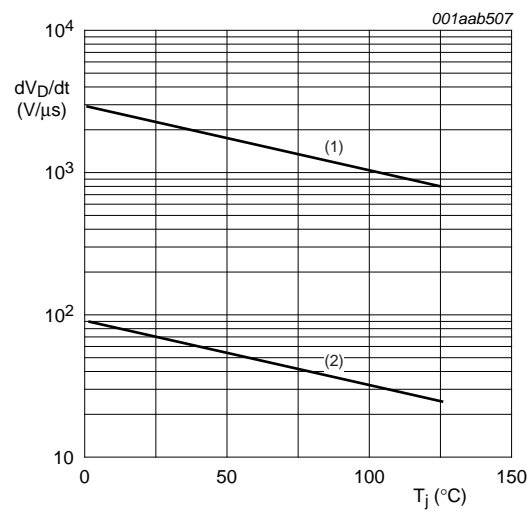


Fig 11. Normalized gate trigger voltage as a function of junction temperature



(1) $R_{GK} = 1 \text{ k}\Omega$ (2) Gate open circuit

Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

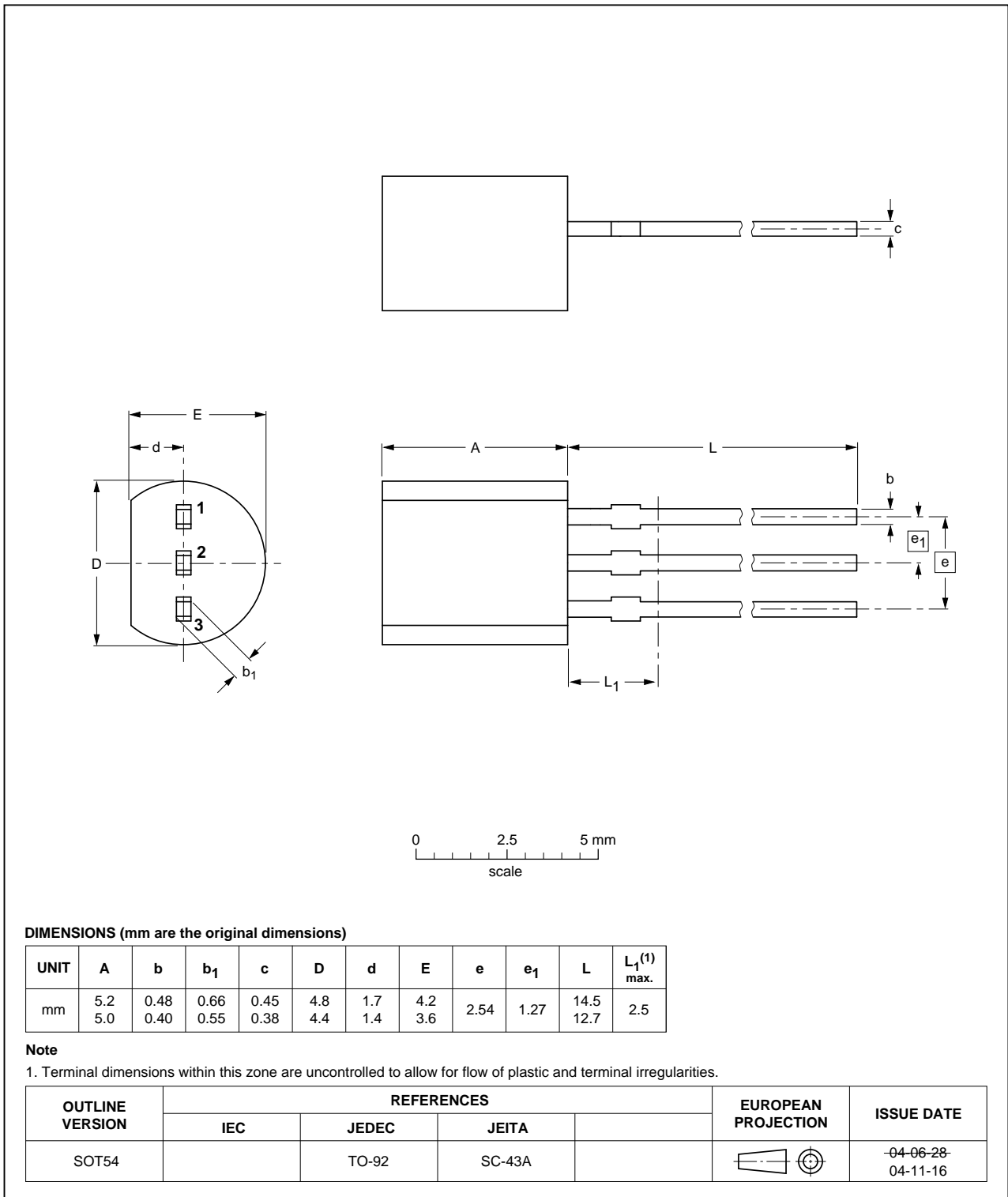


Fig 13. Package outline SOT54 (TO-92)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT169D-L v.6	20120320	Product data sheet	-	BT169D-L v.5
Modifications:	• Various changes to content.			
BT169D-L v.5	20111110	Product data sheet	-	BT169D-L v.4

9. Legal information

9.1 Data sheet status

Document status ^[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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